Test and Optimization of a flexible COME & KISS QDC and TDC for PMT, Si-PM and Diamond Detector Applications

Test und Optimierung eines flexiblen COME & KISS QDC und TDC für PMT, Si-PM und Diamant Detektor Anwendungen

Master-Thesis von Adrian Rost

Tag der Einreichung:

1. Gutachten: Jun.-Prof. Dr. Tetyana Galatyuk
2. Gutachten: Dr. Wolfgang Koenig

TECHNISCHE UNIVERSITÄT DARMSTADT

Fachbereich Physik
Institut für Kernphysik
Virtual Photons - Quark Matter

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Darmstadt, den 28. Februar 2016

(Adrian Rost)

Abstract

The already running High Acceptance Di Electron Spectrometer (HADES) at GSI Helmholtzzentrum für Schwerionenforschung GmbH in Darmstadt, together with the planed Compressed Baryonic Matter (CBM) experiment at the Facility for Antiproton and Ion Research (FAIR) will study the macroscopic and the microscopic properties of dense baryonic matter at beam energies up to 11 AGeV. Both experiments will use calorimeter type detectors which will be read out by photomultiplier tubes (PMTs) or by silicon photomultipliers (Si-PMs), respectively.

A Charge-to-Digital-Converter (QDC) and Time-to-Digital-Converter (TDC) based on a commercial FPGA (Field Programmable Gate Array) was developed to read out PMT signals of the planed HADES electromagnetic calorimeter (ECAL). The main idea is to convert the charge measurement of the detector signal into a time measurement, where the charge is encoded in the width of a digital pulse. The PaDiWa-AMPS front-end board for the TRB3 (General Purpose Trigger and Readout Board - version 3), which implements this conversion method, was developed and successfully used in several beam-times performed by HADES. The well-established TRB3 platform serves as data acquisition system and provides the required precision of the time measurements.

The aim of this work is the optimization, test and finalization of the PaDiWa-AMPS board for the HADES ECAL. SPICE simulations in combination with laboratory measurements have been performed in order to optimize the front-end in terms of charge and time resolution, dynamic range and signal-to-noise ratio. The board was extensively tested in the laboratory, but also used during test and production beam-times.

It has been shown that the read-out concept could be used by a variety of detectors, i.e. HADES Hodoscope, CBM PSD and diamond detectors.

Zusammenfassung

Das sich zur Zeit in Betrieb befindende High Acceptance Di Electron Spectrometer (HADES) Experiment am GSI Helmholtzzentrum für Schwerionenfowrschung GmbH in Darmstadt, zusammen mit dem geplantem (CBM) Experiment an der (FAIR) untersucht die mikroskopischen Eigenschaften dichter barionischer Kernmaterie bei Strahlenergien bis zu 11 AGeV. Beide Experiment werden Kalorimeter Detektoren einsetzten welche mit Photomultipliern (PMT) oder Silizium-Photomultipliern (Si-PM) ausgelesen werde sollen.

Ein Charge-to-Digital-Converter (QDC) und ein Time-to-Digital-Converter (TDC), basierend auf Field Programmable Gate Arrays (FPGAs) wurde entwickelt um PMT Signale des geplanten elektromagnetischen Kalorimeters (ECAL) des HADES Experiment auszulesen. Die Idee besteht darin, die Ladungsmessung in eine Zeitmessung umzuwandeln, wobei die Ladung in der Bereite eines digitalen Pulses kodiert ist. Das PaDiWa-AMPS Ausleseboard für das TRB3 (General Purpose Trigger and Readout Board - version 3), welches diese Konvertierungsmethode implementiert, wurde entwickelt und erfolgreich in verschiedenen Strahlzeiten des HADES Experiments eingesetzt. Die bewährte TRB3 Platform wird als Datenakquisition eingesetzt und erledigt die benötigten präzisen Zeitmessungen.

Das Ziel dieser Arbeit besteht in der Optimierung, dem Test und der Finalisierung des PaDiWa-AMPS Ausleseboards für das HADES ECAL. Zur Optimierung der Ausleseelektronik bezüglich der Ladung und Zeitauflösung, dem dynamischen Bereich und dem Signal-Rausch-Verhältnisses wurden SPICE Simulationen in der Verbindung mit Labormessungen durchgeführt. Die Elektronik wurde dazu ausgiebig im Labor getestet, außerdem erfolgreich in Tests und Produktion-Strahlzeiten eingesetzt.

Es konnte gezeigt werden, dass das Auslesekonzept für eine Vielzahl an Detektoren angewendet werden kann, z.B. HADES Hodoscope, CBM PSD und Diamant Detektoren.

Contents

1 The HADES Experiment

In this chapter the physics program of the HADES experiment at the GSI Helmholtzzentrum für Schwerionenforschung GmbH in Darmstadt is shortly motivated. An overview of the HADES detector system and its general read-out scheme is given. Special emphasis in this work is put on the electromagnetic calorimeter, which is planned to be installed in 2017-2018. The Start-Veto-Hodoscope system which used the read-out concept during the last pion beam experiment in 2014 will be discussed.

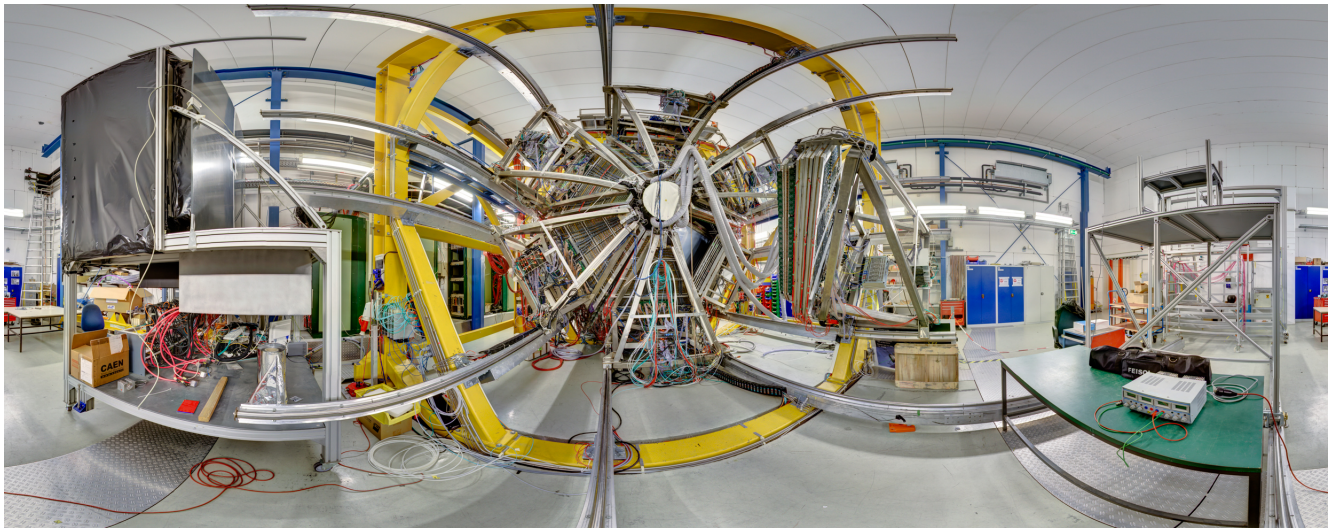


Figure 1.1: A 360° cylindrical panorama composite of the HADES experimental cave at GSI Helmholtzzentrum für Schwerionenforschung GmbH which was taken from its back side. On the left side one can see the Forward Hodoscope Wall which is parked at the side. Each detector subsystem of HADES is segmented into six trapezoidal sectors which are carried by a yellow painted steel support structure. One sector consisting of PRC and Pre-Shower detector is pulled out into service position. The shiny blue foil behind belongs to a sector of the MDC detector. Several kilometers of read-out, sensor and power cables are laid. (December 2014)

1.1 The HADES Physics Program at SIS18 at GSI and SIS100 at FAIR

The ***H**igh **A**cceptance **DiE**lectron **S**pectrometer* (HADES) [1] is in operation at GSI Helmholtzzentrum für Schwerionenforschung GmbH in Darmstadt since the beginning of 2000. The main goal of the HADES collaboration is to study the properties of baryonic rich matter ($\mu_B \cong 700\,\mathrm{MeV}$) at moderate temperatures ($T \leq 100\,\mathrm{MeV}$). The spectrometer has been designed as a fixed target experiment at the SIS18 (heavy ion synchrotron, 18 Tm rigidity) to measure the in-medium masses and widths of the light vector mesons ρ, ω and ϕ via their decay into e^+e^- pairs. Vector mesons are perfect candidates to investigate baryonic matter in the densest phase of a heavy ion collision, the so called fireball. On one hand their lifetimes are short ($\tau_\rho = 1.32\,\mathrm{fm/c} = 0.44 \cdot 10^{-23}\,\mathrm{s}, \tau_\omega = 23.4\,\mathrm{fm/c} = 0.78 \cdot 10^{-22}\,\mathrm{s}, \tau_\phi = 46.5\,\mathrm{fm/c} = 1.55 \cdot 10^{-22}\,\mathrm{s}$ [2]) compared to the duration of the compression phase in a heavy ion collision ($\tau_{\mathrm{fireball}} = 10\,\mathrm{fm/c} = 3.34 \cdot 10^{-23}\,\mathrm{s}$ [3]). Furthermore, the light vector mesons can decay electromagnetically into lepton pairs (e^+e^-, $\mu^+\mu^-$) which do not interact via the strong interaction. Consequently di-electrons can be used as perfect probes for the dense baryonic matter under extreme conditions.

The HADES has been originally optimized to measure di-electrons. Due to the high precision of time-of-flight and energy loss measurements the HADES is also an excellent detector to measure hadrons. For this reason emphasis is also on the production and propagation mechanism of particles containing strangeness.

The physics program of the HADES collaboration is focused on beam energies of 1 - 3.5 GeV at SIS18. Currently the possibilities of di-electron measurements in heavy ion collisions are exploited up to Au+Au collisions at the energy of 1.25 AGeV.

Besides the heavy ion program also pp, pA and πp collisions are under investigation [4]. The most recent experiment using a secondary pion beam took place in Summer 2014. These experiment provide a unique chance to study the coupling of virtual photons to barionic resonances by means of the reaction $\pi N \rightarrow R \rightarrow e^+e^-N$. Besides that one could study strangeness ($K^{\pm}, K^0_S, \phi$) production in π-nucleus reactions, one- and two- pion production channels in π^-p reactions, Kanon-Hyperon production in π^-p reactions.

At future SIS18 operations the HADES experiment will profit from an ***E**lectromagnetic **Cal**orimeter* (ECAL) upgrade. It is foreseen to replace the Pre-SHOWER detector by an ECAL detector in order to measure π^0 and η mesons via their two photon decay. Also ω vector mesons can be reconstructed via their decay channel $\omega \rightarrow \pi^0\gamma \rightarrow \gamma\gamma\gamma$, as well as direct photons and photons coming from decays of neutral $\Lambda(1405)$ and $\Sigma(1385)$ resonances. In Fig. 1.2 (left panel) the $M/|q|$ times polarity as a function of particle momentum p, reconstructed with the RPC detector is shown. An additional ECAL will significantly improve the electron/pion separation at large momenta ($p > 400$ MeV/c).

At SIS100 (heavy ion synchrotron, 100 Tm rigidity) operations, at the planned ***F**acility for **A**ntiproton and **I**on **R**esearch* (FAIR) in Darmstadt, the HADES spectrometer will be placed on a platform in front of the ***C**ompressed **B**aryonic **M**atter* (CBM) experiment (see Fig. 1.2 (right panel)). The HADES experiment will continue its physics program especially at collision energies from 2 to 11 AGeV, the CBM experiment will be able to measure very heavy systems at maximal energies up to 14 AGeV.

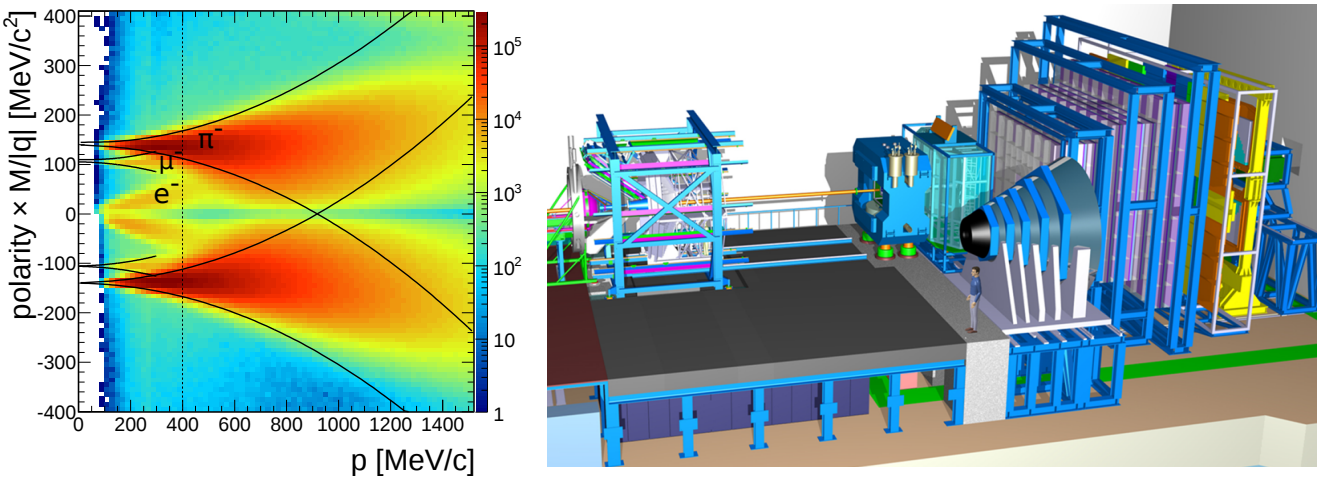


Figure 1.2: Left panel: $M/|q|$ times polarity as a function of particle momentum p reconstructed with the RPC detector. Electron/pion separation at large momenta can be improved by including an electromagnetic calorimeter (ECAL) into the HADES set-up. **Right panel:** Artist view of the experimental cave housing the HADES and the CBM experiment at the future FAIR accelerator complex [5].

1.2 The HADES Set-up - Present and Future

The HADES covers polar angles from 18° up to 85° and nearly the full azimuth angular range of 360°. The track reconstruction efficiency is 90% (for particles with momenta $> 100\,\mathrm{MeV/c}$) and a mass resolution in the vector mesons region ($\mu_{ee} \cong 800\,\mathrm{MeV/c^2}$) is $15\,\mathrm{MeV/c^2}$. The identification of electrons, pions, kaons, protons and light nuclei is possible by means of time-of-flight, momentum and energy loss measurements. To reduce background from conversion of photons into di-electron pairs inside the spectrometer all tracking-detectors have been designed as light as possible. Most detector layers of the HADES consist out of six trapezoidal sectors which are put together to a hexagon. A transverse section view of the detector layout is shown in Fig. 1.3. The main detector components are a Start-Target-Veto and Hodoscope System, a Ring Imaging Cherenkov Detector (RICH), four planes of Multiwire Drift Chambers (MDC), two in front and two behind of an Iron Less Superconducting Electro Magnet (ILSE). As well a META (Multiplicity- Electrons- Trigger-System) detector consisting of a Resistive Plate Chamber (RPC), a scintillator based Time of Flight Wall (TOF), a Pre-Shower detector and a Forward Hodoscope Wall is used for Event Plane reconstruction and centrality determination. It is foreseen to replace the Pre-Shower detector by an Electromagnetic Calorimeter (ECAL) in 2017. A high performance Data Acquisition System (DAQ) which deals with 100 000 individual front-end channels reaches 100 kHz (p+p) and 20 kHz (Au+Au) event rate and up to 400 MBytes/s data rate. In the following subsections each detector will be shortly described. Particular emphasis will be given to the Start-Target-Veto and Hodoscope System and the ECAL detector because those detectors are read-out using the concept which will be introduced in chapter 2.

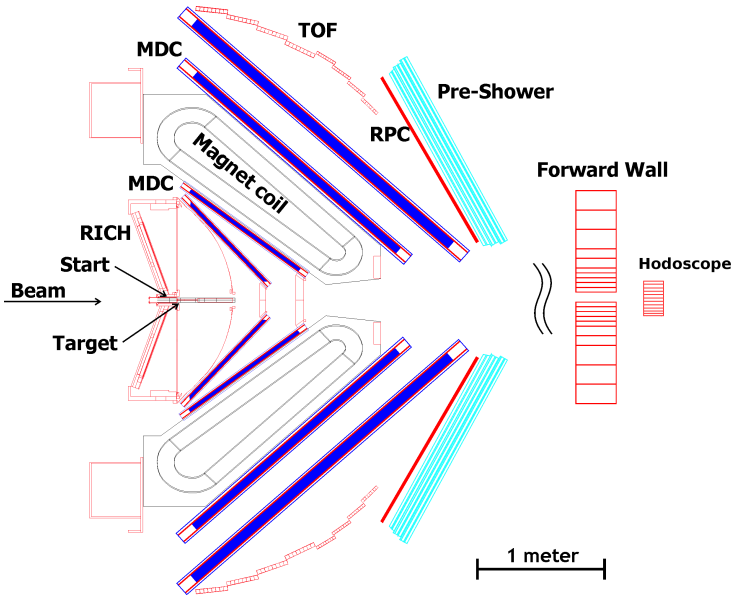
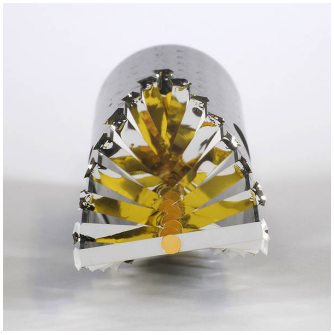


Figure 1.3: Transverse section view of the HADES detector layout as it was used during the pion beam experiments in Summer 2014. As already mentioned the Pre-Shower detector will be replaced in future by an Electromagentic Calorimeter (ECAL) [6].

Start-Target-Veto and Hodoscope System

Experiments using solid fixed targets as KCl, Carbon, Niobium, Wolfram, Gold, Polyethylene and also with a liquid hydrogen target have been performed. To reduce unwanted gamma conversion and multiple scattering in the target the solid targets are segmented into several slices. For example the Gold target which was used in the Au+Au beam time in 2012 was segmented into 15 segments with a thickness each of 25 μm. The interaction probability is in the order of a percent. The target foils are glued

on a Kapton® polyimide film which are mounted in a carbon fiber support frame. This construction is located in the beam-line inside the RICH. In Fig. 1.4 (left panel) the segmented gold target of the Au+Au run in 2012 is shown.



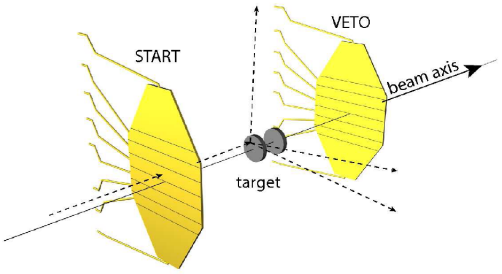
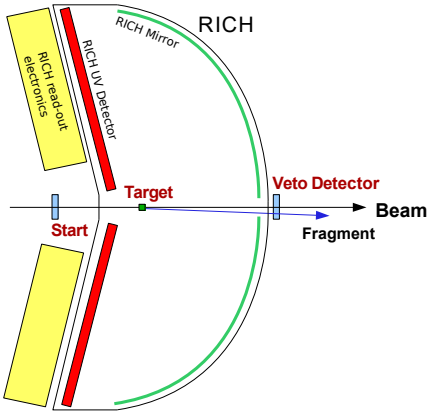


Figure 1.4: Left panel: Photography of the Gold target which was used in the HADES Au+Au beam time in 2012. It is segmented into in 15 segments, with a thickness of 25 μm, which are mounted in a carbon fiber support. (Picture by Gabi Otto, GSI) **Right panel:** Schematic view of the Start-Target-Veto System as it was used in the same Au+Au beam time [5].

In front of the target a diamond based Start detector [7, 8] is placed to get the t_0 "start" signal which is used for the time-of-flight measurements in the HADES. It is also used together with the multiplicity trigger array (META) to trigger on high multiplicity events. A second diamond based Veto detector is placed behind the target with the purpose to "veto" beam particles which did not interact with the target. Both diamond detectors are made from mono-crystalline scCVD (single crystal Chemical Vapour Deposition) diamond material which became industrially available in the last years. The diamond material is metallized with a thin layer of chrome and gold, which is usually in the order of 50 to 150 nm, to provide reliable contacts between the diamond and the metal electrodes.

Charged particles traversing the diamond material produce free electron-hole pairs. The number of electron-hole pairs is proportional to the energy deposited in the diamond. Some electrons are transferred from the valence band to the conductor band and an equal number of holes are created in the valence band. A high voltage on the order of 300 V provides an electrical field which forces the electrons and holes to move to the electrodes. The very high drift velocities of electrons and holes in diamond material, in comparison to semiconductor material, results in excellent timing properties. Besides radiation hardness, diamond material offers other desired properties like: wide-band-gap, high breakdown voltage, high thermal conductivity and small dielectric constant which are very attractive for beam detectors. The thickness of the diamond detector has to be chosen depending on the energy loss of the beam particles and is in the order of 50 μm to 300 μm. The number of electrons arriving at the electrodes is proportional to the deposited energy and can be measured by a dedicated read-out circuit. The generated voltage pulses are usually very small and a pre-amplification is needed. To reduce external noise the pre-amplification stage should be done as close as possible to the diamond. In Fig. 1.5 (right panel) a diamond detector and the first pre-amplification stage is shown. The electrodes are bonded directly to a printed circuit board (PCB) with a first pre-amplification located very close. By segmenting the diamond also position information can be obtained which is useful for beam diagnostic purposes. This allows the monitoring of the position and the quality of the beam in front of the target. Currently diamond detectors in HADES are read-out by the a fast discriminator ASIC, based on the NINO chip [9], in combination with the TRB3 [10]. It is planed to adapt the read-out concept, which will be introduced in this work, also to diamond detectors (see section 6.1.2).

During the HADES pion beam time in summer 2014 a Hodoscope detector [12] was used as an additional beam position monitoring system. The CERBEROS pion tracking system [13] which consist of two silicon based tracking detectors, the Start and the Hodoscope detector was used to reconstruct the pion



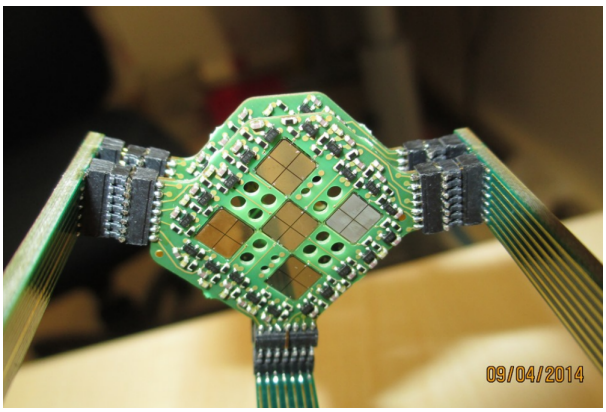


Figure 1.5: Left panel: Schematic picture of Start and Veto diamond detectors and the Target which are placed in the RICH detector. The distance between Start and Veto detector is about 0.5 m. The Hodoscope beam detector (not shown) is placed about 6 m downstream the target [11]. **Right panel:** Diamond based Start detector which was used in the pion beam experiment in 2014. It was made from 9 mono-crystalline CVD diamonds with a thickness of $300\,\mu$ and a size of $4.6x4.6\,\mathrm{mm}^2$ each. Due to a clever arrangement of the diamonds a total area of $1.9\,\mathrm{mm}^2$ can be covered. The diamonds are directly attached to a PCB. A first pre-amplification stage is positioned as closed to the detector to reduce electronics noise. (Picture by Jerzy Pietraszko, GSI)

momentum and do beam tracking from the pion production target to the HADES target, but also inside the HADES. The Hodoscope was located about 6 m downstream the target to provide at theta angles below 2° position and time information for beam particles. The Hodoscope was restored from a previous pion beam time and tested at the Nuclear Physics Institute (NPI) of the ASCR in Řež, Czech Republic [6]. It consist of eight 10x5x100 mm Bicron BC404 plastic scintillator rods which are horizontally aligned. On both ends of the rods the scintillation light is guided through light guides to 0.5 inch HAMAMATSU R3478 photomultiplier tubes (PMTs). In Fig. 1.6 a photography and a schematic drawing of the Hodoscope are shown. The y-resolution is defined by the dimensions of the rods, x-position information can be obtained by considering the arrival time of the scintillation light in the PMTs at both ends of the rods.

The read-out concept which will be described in detail in chapter 2 was used for time and charge measurement of the analog PMT pulses. The front-end electronics had to be optimized for the Hodoscope PMT pulses.

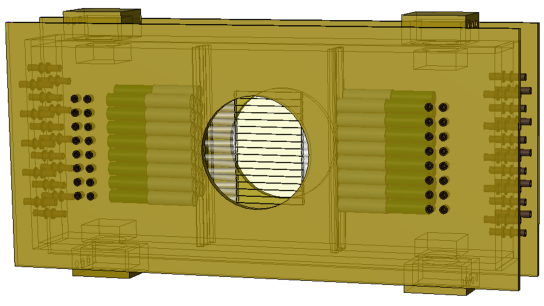


Figure 1.6: Schematic drawing (left panel) and photography (right panel) of the Hodoscope detector which belongs to the beam diagnostics system of the HADES. The Hodoscope consist of 16 horizontally aligned plastic scintillator rods. The scintillation light is read out at both ends by PMTs. The system is mounted in a light tight plastic housing [14].

RICH Di-electron Identification Detector

The **R**ing **I**maging **CH**erenkov (RICH) detector [15] is the central detector for the identification of electrons and positrons. They are created among others by the decay of light vector mesons. This is a quite rare process, i.e. for ρ meson the branching ratio into a di-electron decay is $4.72 \cdot 10^{-5}$. The physical process which is used in the RICH detector is the Cherenkov effect. A charged particle traversing a radiator gas with a velocity faster than the velocity of light in the gas is emitting Cherenkov-photons in a Mach cone. Here C_4F_{10} is used as radiator gas. The Cherenkov cone is reflected by a spherical ultraviolet mirror and ring images are focused on the photon detector which is separated from the radiator gas by a CaF_2 window. The photon detection system consist of about 28 000 CsI photo cathode pads glued to a mounting frame. Cherenkov photons undergo the photo-electric effect and the released electrons are accelerated by an electrical field. That creates an avalanche which is detected in a multi-wire proportional chamber. The ions are caught by the cathode pads. The mirror is made out of 18 pieces with full azimuth coverage of 360°. Due to the mirror diameter of 145 cm, theta angles between 18° and 85° are covered. In Fig. 1.7 (left panel) the schematic structure and the operation principle is shown. In the data analysis one is searching for ring images on the CsI pads. In Fig. 1.7 (right panel) a typical response pattern with two possible ring candidates is shown. It is planed to upgrade the RICH photon detection system in near future. To achieve intensity of the ring images new HAMAMATSU multi anode photomultiplier tubes (MAPMTs) will be used to detect the Cherenkov photons.

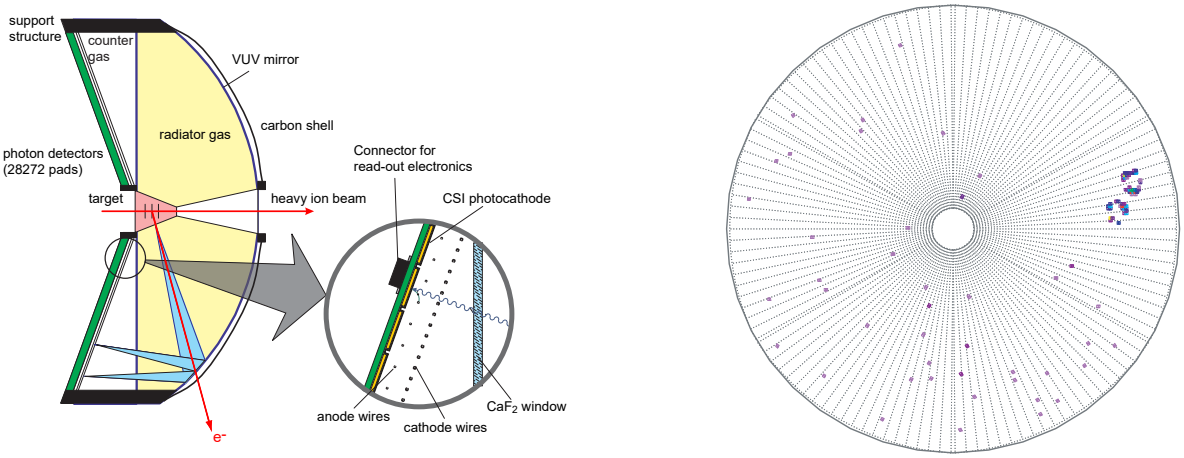


Figure 1.7: Left panel: Schematic drawing of the RICH detector. The Cherenkov cone of an electron (the same hold for positrons) is focused by a spherical mirror on the photon detection system. The photon detection system consists of about 28000 photo cathode pads. Released photoelectrons are amplified and detected in a multi-wire proportional chamber. [16]. **Right panel:** Typical response pattern of the CsI pads in a heavy ion collision. Two possible ring candidates are visible on the right side [17].

Magnet Spectrometer - MDC Tracking System

The tracking system [18] for charged particles consists of four planes of **M**ultiwire **D**rift **C**hambers, historically called **M**ini **D**rift **C**hambers (MDCs), in combination with a superconducting magnet. It allows charged particle tracking and momentum reconstruction by measuring the deflection angle of particles traversing the magnetic field. It is also possible to identify charged particles by energy loss measurements inside the chambers. The magnet consist of six superconducting NbTi coils which produce a toroidal magnetic field with a gradient from 3.6 T at the coil surface to 0.8 T in the center. In Fig. 1.8 (left panel) the schematic front view of the super-conducting magnet is shown. In Fig. 1.8 (right panel) a

field map of the magnetic field and a positively charged particle track is shown. Two MDC planes (MDC I, MDC II) are located in front of the magnet and two behind it (MDC III, MDC IV). Polar angles between 18° and 85° are covered. Each drift plane consists of six MDC chambers. A chamber is composed out of six layers of drift cells. In Fig. 1.9 (right panel) a schematic picture of a drift cell is shown. A single drift cell consists out of two layers of cathode wires aligned in y direction. Two field wires which are made of Al with a thickness of 100 μm provide an electrical field. A Gold plated Tungsten sense wire with a thickness of 20 μm is used as an anode in between the field wires. The field and sense wire planes have an orientation of 0°, 20° and 40° with respect to the normal on the symmetry axis of the module for maximum spatial resolution in polar direction. In Fig. 1.9 a MDC chamber is shown with the orientation of the field and sense wire planes. In MDC I a mixture of Argon and $C0_2$ (70% : 30%) and in MDV II to IV a mixture of Argon and Isobutane (84% : 16%) is used as counting gas in the cells. A traversing charged particle ionizes the counting gas. Electrons are accelerated towards the sense wires. Close to the wires the electric filed is high and an avalanche is created. The chambers are equipped with dedicated read-out mother and daughter boards which are mounted onto the detector. The daughter boards contain a preamplifier, a shaper and a discriminator. The motherboards itself contain the Time-to-digital Converters (TDC). For the future an upgrade of the electronics is planned. With the current set-up a momentum resolution of about 1% can be achieved.

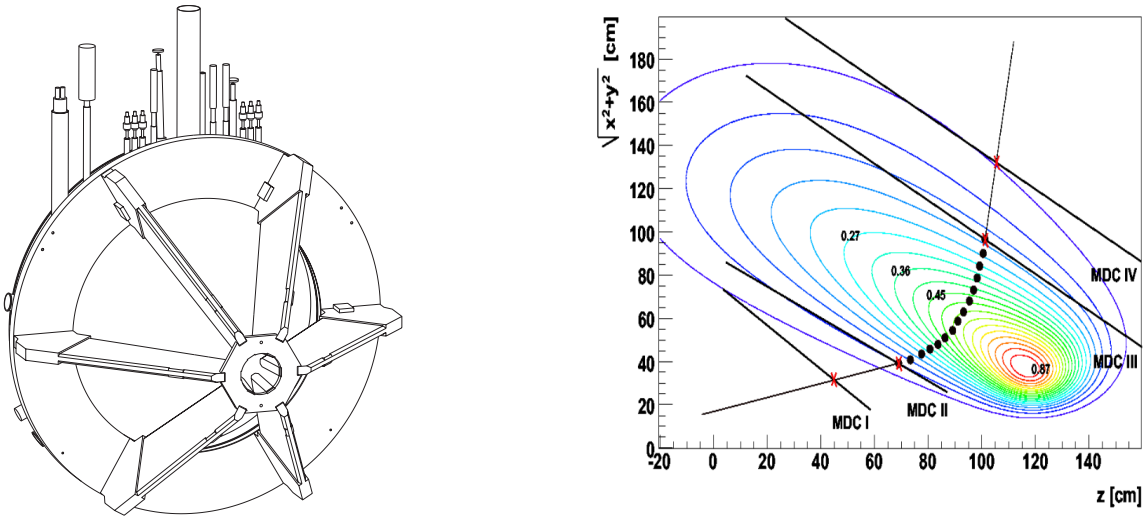


Figure 1.8: Left panel: Schematic picture of the HADES magnet. The diameter of the outer ring is 3.56 m. The pipes on top are used for inflow and outflow of the liquid Helium which is used for cooling. Also power and sensor cables are guided by the pipes [1]. **Right panel:** Particle trajectory of a negative charged particle which experienced the Lorenz force due to the magnetic field. The particle is tracked in all four MDC sections. The magnetic field map shows B as function of z (along beam axis) and r (perpendicular to the beam axis), at $\Theta = 0$ (mid-plane between coils). The step size for the contour lines is 0.046 T [1].

Time of Flight Wall

A **T**ime **o**f **F**light Wall (TOF) [19] is placed in the region behind the tracking system and covers outer polar angels between $44° < \Theta < 88°$. It is used for time-of-flight measurements in combination with the Start detector. It also provides the trigger signal for the HADES Data Acquisition (DAQ). The combination of the time-of-flight measurement with momentum determination provided by the tracking system and the energy-loss measurement permits to perform efficient particle identification. The TOF detector follows the six sector structure of the HADES. Each sector consists of 48 plastic scintillation rods which are arranged in sets of eight modules enclosed in a carbon fiber case. The rod cross section is

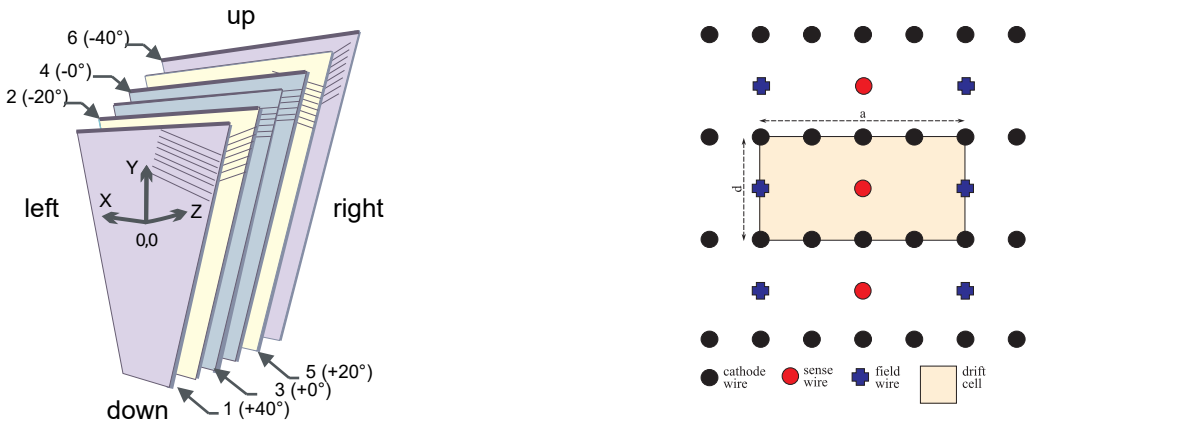


Figure 1.9: Left panel: A HADES MDC chamber which is made out of six layers of Multiwire Drift Chambers. The different inclinations of layers of sense and field wires are shown. All cathode wires are aligned in y direction and are not shown [1]. **Right panel:** The relative position of sense and field wires are shown in the x-y plane. The definition of the MDC drift cell, which extends out of and into the drawing plane to form a long box centered around the sense wire and delimited by the field wires and the cathode wires, is shown. Note that the angle between the cathode wires and the drift cell which is given in the left figure is not shown [5].

$20\times20\,\mathrm{mm}^2$ for the innermost 192 rods and $30\times30\,\mathrm{mm}^2$ for the outermost 192. The rod length varies from 1 m to 2 m, respectively, from smaller to larger polar angles. Each rod is made of Bicron BC408 plastic scintillator material. The end of the rod is glued to a light guide, which are bent by 70° with respect to the rod itself and coupled to Electron Tubes Limited 9133B PMTs. Charged particles traversing the plastic scintillator are generating scintillation light. The rod itself is used to guide the scintillation light to the photomultiplier on both ends. From the arrival time of the signal to the PMT the x-position can be calculated. The position resolution in y-direction is given by the dimension of the scintillation rods and is in the order of 2 - 3 cm.

The electronic chain includes a NINO chip [9] based leading edge discriminator and a Time to Digital Converter (TDC). Charge information can be obtained by a charge-to-width method.

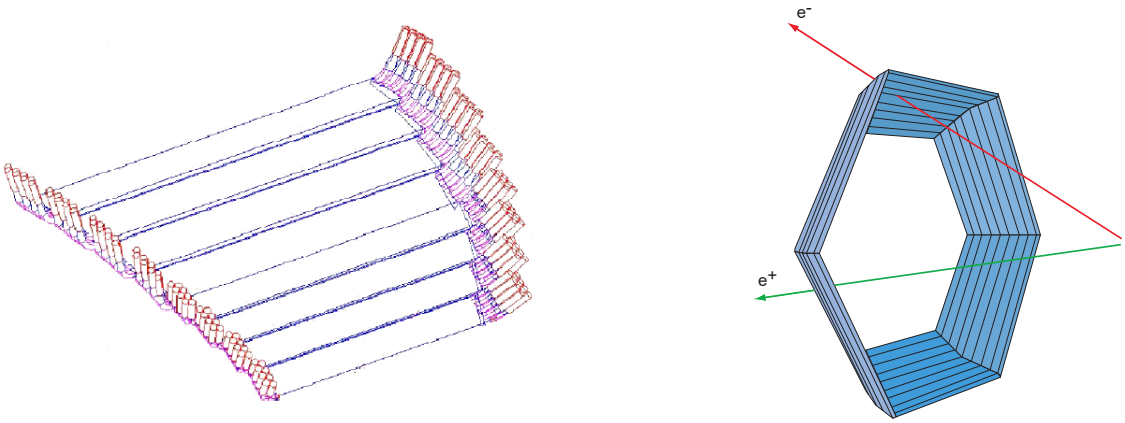


Figure 1.10: Left panel: Schematic layout of one sector of the Time of Flight Wall consisting of eight boxes of plastic scintillator stripes. The strip width is decreasing at lower polar angles to deal with the higher particle flux. Scintillation light is guided to the ends of the stripes were light guiders transport the light to the PMTs [5]. **Right panel:** Layout of the TOF detector showing the detection of an electron and a positron in two different sectors [5].

Resistive Plate Chamber Detector

A **R**esistive **P**late **C**hamber (RPC) [20] is used for time-of-flight measurements at forward polar angles between 18° and 45°. It is built out of six RPC sectors. Each sector consists of two layers of overlapping RPC cells with different length. In total 1116 cells are installed. A single RPC cell consists out of a sandwich of three Aluminum and two glass electrodes which carry a potential of 5 kV. They are enclosed in an Aluminum box. The cell is filled with a gas mixture of SF_6 and $C_2H_2F_4$. The cell layout of the The HADES RPC and a schematic drawing of a RPC sector is shown in Fig. 1.11.

A charged particle traversing the detector ionizes the gas atoms along the track. The applied high potential difference between the electrodes accelerates the produced electrons and ions, thus more gas atoms are ionized. An avalanche is created, which leads to a discharge of the electrodes. Because of the high resistivity of the glass electrodes, the electric field near to the discharge is suddenly switched off. Hence the discharge is prevented from propagating through the whole gas. Consequently the RPC is only blind in a small area near to the discharge and the other parts of the detector are still fully operational. The gas mixture is chosen to absorb the ultraviolet part of light to inhibit secondary discharges. The following relaxation time for the blind spot is typically in the order of ms. This allows a high rate capabilities of RPC detectors. Due to the change of the electric field in the region of the discharge, a signal is induced. By combining several RPC layers to a so called multi-gap RPC the efficiency, the rate capability and the time resolution can be improved. The main feature of the HADES multi-gap RPC designs is that each individual cell is electrical shielded. That allows an excellent multi-hit capability.

The RPC cells are read out on both sides via a DaughterBOard (DBO) and a dedicated MotherBOard (MBO). The DBO uses a fast 2 GHz amplifier feeding a discriminator. The time and the charge information are encoded in the leading and the trailing edge of an LVDS signal by a charge-to-width method. The LVDS signals are sent to the TRB2 [21] readout MBO with time-to-digital converter capability. Time resolutions which can be achieved with the HADES RPC are in the order of 70 ps.

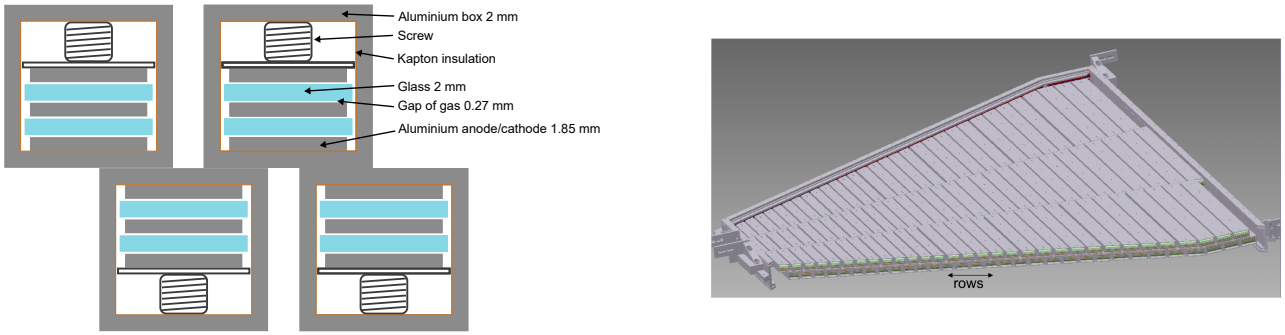


Figure 1.11: Left panel: The HADES multi-gap RPC cell layout and their ingredients. The cells are aligned in two overlapping rows [22]. **Right panel:** A schematic drawing of a RPC sector. The cells have smaller sizes at smaller polar angles and fill the trapezoidal support frame [5].

Pre-Shower Detector

The **Pre-Shower** detector [23] is mounted behind the RPC detector and covers polar emission angles from 18° to 44°. It is used for electron identification by measuring electromagnetic showers produced in lead converter material. It consists of two lead converters inserted between three wire chambers with pad read-out. Shower recognition is performed by comparing the number of particles measured before and after the lead converters. Particle hits are identified via the charge produced in ionization processes in the wire chambers which are working in the self-quenching streamer (SQS) mode. The main advantage of the SQS mode is that induced charge is nearly independent of particle specific energy loss and therefore low energy protons do not produce large signals in the post converter chambers because

of their significant energy loss in the lead material and finally are not misidentified with electromagnetic showers. In Fig. 1.12 (left panel) the shower generation for an electron and a proton is schematically shown. In Fig. 1.12 (right panel) a schematic drawing of the arrangement of the wire chambers is shown. They are arranged into 32 rows per chamber. The read out is performed with front-end electronics boards, based on a dedicated ASIC chip. The ASIC chip contains a 32-channel charge amplifier and signal shaper with output multiplexer, and digitization with an 8-bit ADC.

As already mentioned for future experiments the Pre-Shower detector will be replaced by an Electromagnetic Calorimeter. The update planes are described in the Electromagnetic Calorimeter section.

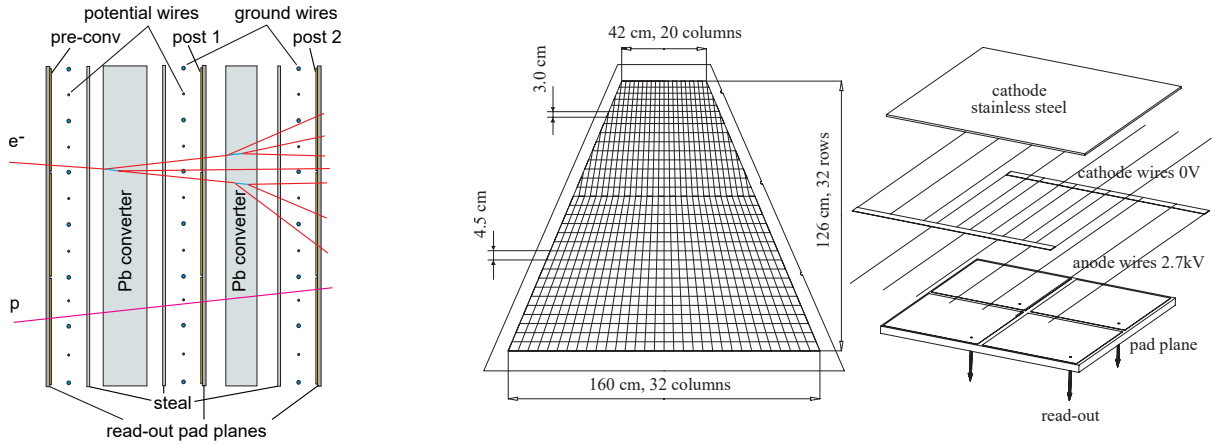


Figure 1.12: Left panel: Schematic side view drawing of the Pre-Shower Detector. An electromagnetic shower produced by an electron is much more pronounced than a hadronic shower induced by a proton [1]. **Right panel:** Schematic drawing of a wire chamber which is used to detect the shower which are created in the lead material [1].

Forward Hodoscope Wall

For measurement of the centrality and the reaction plane of a heavy ion collision a Forward Hodoscope Wall [24] is used. The detector is located 7 m downstream the target and covers polar angles from 0.22° up to 7°. It is made out of 228 scintillation modules which are read out by PMTs. The szintillator modules have three different cell sizes with 4x4 cm, 8x8 cm and 16x16 cm. A schematic front view of the Forward Hodoscope Wall is shown in Fig. 1.13.

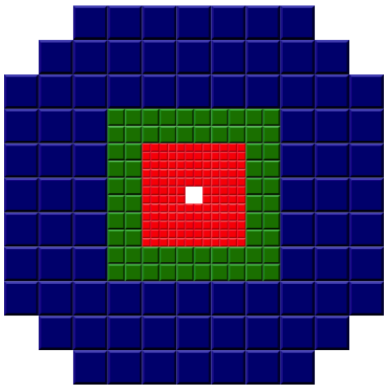


Figure 1.13: Schematic front view of the Forward Hodoscope Wall. The detector is made out of 228 plastic scintilation cells in three different dimensions which are indicated by the colors blue, green and red which are read out by PMTs [5].

The **ECAL** [25–28] detector will be built from 978 lead glass modules which are read out by PMTs. The modules will be arranged in six sectors, mounted on a movable support structure on a rail system. It will cover almost full azimuths and polar angles from 12° to 45°. The design energy resolution for photons and electrons is about $6\%/\sqrt{E[\mathrm{GeV}]}$. A 3D model of the HADES ECAL detector is shown in Fig. 1.14 (left panel).

Each HADES ECAL module consists of a modified lead glass module obtained on loan from the OPAL End-Cap calorimeter at CERN [29][30]. Lead glass (Corning CEREN 25) is used as a Cherenkov radiator. The glass has a density of $\rho = 4.06\,\frac{\mathrm{g}}{\mathrm{cm}^3}$, a refraction index of $n = 1.708$ (at 410 nm) and a radiation length of $X_0 = 2.51$ cm. All modules have the same length of 420 mm (16.7 radiation lengths). The transverse size of $92 \times 92\,\mathrm{mm}^2$ is comparable to the transverse size of the expected electromagnetic showers. A light tight brass box with a thickness of 0.45 mm is used as a housing for the module and the PMT and its high voltage divider (HV-divider). For detection of the Cherenkov light a PMT is connected to one side of the lead glass block via optical grease (RHODORSIL Paste No. 7). All sides of the block are mirror polished and wrapped in Tyvek® to reduce lateral escape of photons. An optical fiber is coupled to the lead glass block with a standard optical link connector on the end plate. This allows putting external LED light into the module for calibration and monitoring purposes. A schematic view of an ECAL module is shown in Fig. 1.14 (right panel).

In lead glass the Cherenkov effect is used to determine the deposited energy. Gamma photons or fast charged particles which enter the lead glass produce an electromagnetic shower, which consist mainly of electrons, positrons and gammas. Charged particles may travel through the lead glass at a speed greater than the velocity of light in that medium and produce Cherenkov radiation. The number of Cherenkov photons is proportional to the deposited energy [31]. The Cherenkov light is then detected by a Photomultiplier Tube (PMT). The charge of the pulse is then directly proportional to the deposited energy.

Until recent there have been several considerations for different PMTs with photo cathode sizes ranging from 1 up to 3 inch. Tests were done using a 1.5 inch EMI 9903KB, 1 inch HAMAMATSU R8619 (with HV-divider H10580) and 3 inch HAMAMATSU R6091 (with tapered HV-divider H6559) PMTs. The performances of the PMTs in combination with the lead-glass have been deeply investigated in a photon beam time at the MAMI facility in Mainz in 2014. Detailed results will be presented in chapter 5.

A very important parameter of a calorimeter is its energy resolution, which is defined as the following sum:

$$\left(\frac{\sigma_E}{E}\right) = \left(\frac{a}{\sqrt{E}}\right) \oplus \left(\frac{b}{E}\right) \oplus (c), \tag{1.1}$$

where a characterizes the photoelectron statistic (stochastic term), b characterizes the noise of the read-out electronic and c characterizes the possible uncertainty in the calibration. The OPAL experiment measured an energy resolution of

$$\frac{\sigma_E}{E} = \frac{5\%}{\sqrt{E[GeV]}}, \tag{1.2}$$

in which the stochastic term is dominant [30]. However, after several years of operation in a high radiation environment the energy resolution needs to be investigated again. This also motivated a gamma beam time at the MAMI facility.

The read-out electronic should be able to provide a precise time and charge measurement of the PMT pulses. The PMT pulses have a full rise-time of 3 ns and a full fall-time of 50 ns. Typical pulse shapes for a gamma photon beam with different energies are shown in Fig. 1.15. A dynamic range of 50 mV - 5 V should be measurable with an accuracy of 5 mV. The required time resolution is 500 ps. The expected hit rate is about 10 kHz/channel. It should also be easy to integrate the electronics into the HADES read-out

scheme. In chapter 3 it will be shown, that the newly developed read-out concept will fulfill all above mentioned requirements.

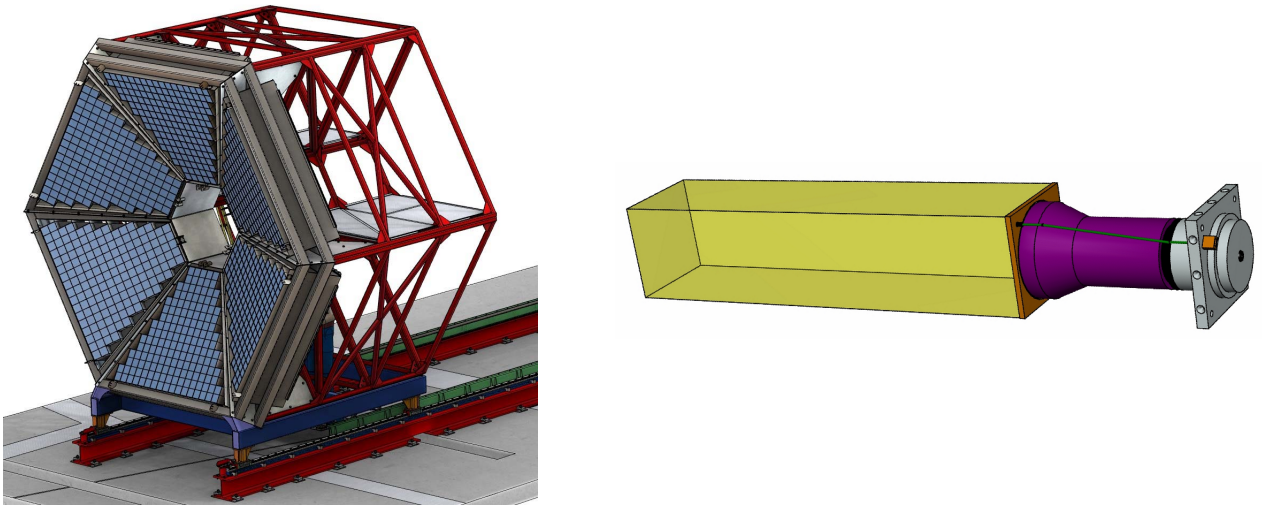


Figure 1.14: Left panel: 3D model of the HADES ECAL detector with about 1000 lead glass modules [25]. **Right panel:** Components inside an ECAL module consists of a lead glass block (yellow) coupled to a PMT (magenta). LED light for testing purposes can be inserted via an optical fiber (green). The lead glass is warped in Tyvek and a light tight brass box is used as housing (not shown) [14].

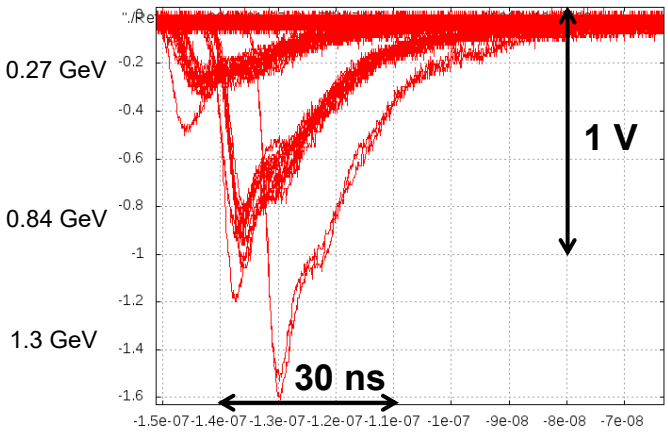


Figure 1.15: Typical pulse shapes from an ECAL module, recorded with an oscilloscope. The module was equipped with a 3 inch HAMAMATSU R6091 PMT and irradiated with three different gamma energies. Important for the adaption of the read-out electronics is the rise-time (about 2.5 ns), the fall-time (about 40 ns) and the dynamic range of the amplitude.

HADES Data Acquisition Network

All sub-detectors of the spectrometer are connected to the HADES **D**ata **Acq**uisition (DAQ) network [32]. A common network set-up was chosen to simplify development, integration and maintenance. The DAQ network consists of two main parts. The first part is an FPGA based custom network, the so called TrbNet [33] network, with optical links inside the detector. The second part is a commercial Gigabit Ethernet (GbE) infrastructure for transporting the digitized detector data to the server farm. A schematic sketch

of the tree-like structure of the HADES DAQ network is shown in Fig. 1.16 (left panel). All detectors are connected to the Central Trigger System (CTS) which controls the trigger and the read-out process. Several types of data and information are transported in parallel using the TrbNet network setup. For that the network is divided into three virtual channels. The first channel is used for the distribution of the Level1 (LVL1) trigger signal which has the highest priority. It communicates the trigger information from the CTS to all data collecting front-ends. Once the trigger information packet is transmitted, the channel remains blocked until all front-end endpoints have returned a busy-release packet. After a trigger cycle is completed, the CTS has to instruct all front-end endpoints to send their data. This is done in a second TrbNet channel. The Event Data is requested from the CTS and transferred via GbE to the Eventbuliders were the data is prepared for permanent storage. The third channel is used for Slow Control of the different detectors and front-end board. A schematic view of the TrbNet network is shown in Fig. 1.16 (right panel). In the last Au+Au beam time in 2012 the DAQ was recording with a trigger rate of 8 kHz and a data rate of 200 MByte/s. In total 140 TByte of data have been recorded by hard disks.

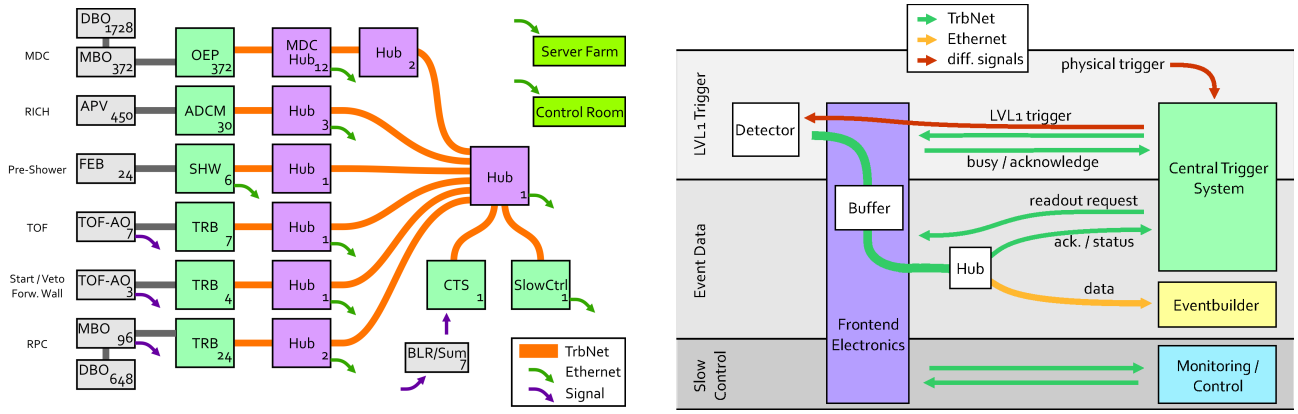


Figure 1.16: Left panel: Schematic view of the tree-like structure of the full HADES TrbNet network setup. All detectors are connected to the central control system. The numbers show the amount of each board type in the HADES setup [32]. **Right panel:** Schematic view of the TRBNet network. Several types of data and information are transported in parallel using one common network setup. The network is divided into three virtual channels. The first channel is used for the distribution of the LVL1 trigger signal. In the second channel the Event Data is requested from the Central Trigger System and transferred to the Eventbulider. The third channel is used for Slow Control of the different detectors and front-end boards [32].

2 The FPGA Based QDC and TDC Read-out Scheme

Particle detectors used in high energy physics experiments need a dedicated read-out and digitization system. It is often needed to extract with a very high precision the arrival time and the amplitude of the signal, the time-over-threshold or the charge of the electric signal pulses generated by the detectors. This information is needed to calculate the particle type, its energy and its momentum which play an important role in the final data analysis of the experiment. There are several approaches to get this information. In the following chapter the basic principles of a Charge-to-Digital-Converter (QDC) and also a Time-to-Digital-Converter (TDC), which are implemented in field-programmable gate arrays (FPGAs), will be explained. The newly developed PaDiWa-AMPS prototype board for the already well established TRB3 platform will be presented. On this board the new QDC concept is implemented. The general read-out concept will be explained.

2.1 Signal Discrimination in FPGAs using the LVDS Input Buffers

The PaDiWa-AMPS front-end board (see section 2.4 for more details) implements among others a discriminator in a Lattice MachXO2-4000HC FPGA. Detailed information about FPGAs one can find in appendix 8.1. The Lattice MachXO2 devices support Low Voltage Differential Signaling (LVDS) outputs via emulation (LVDS25E). This is done by using the Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS) outputs in conjunction with resistors across the driver outputs and inputs. The resistors attenuate the signals from differential LCMOS output drivers and provide matched source impedance to the transmission line as required by the LVDS specification. The scheme shown in Fig. 2.1 (left panel) is one possible solution for an LVDS standard implementation. The LVDS input buffers can be misused for signal discrimination [34] by using them as a comparator. The analog signals are sent to the input buffers and discriminated against a reference voltage. A discrimination threshold can be set by varying the reference voltage of the input buffers. For this a Digital-to-Analog Converter (DAC) is implemented with the help of Pulse Width Modulation (PWM) inside the FPGA. A low pass filter outside the FPGA is used to filter the ripple which is unavoidable generated by the PWM. The signal discrimination scheme is shown in Fig. 2.1 (right panel). The characteristic information of the input pulse is then encoded in the discriminated digital pulse. The arrival time of the input signal is encoded in the leading edge. The time-over-threshold of the input signal is encoded in the width of the digital pulse. Finally the digital pulses can be post processed inside the FPGA or can be sent out as differential signals via the LVDS output buffers to a Time-to-Digital-Converter (TDC) for time measurements (see section 2.2).

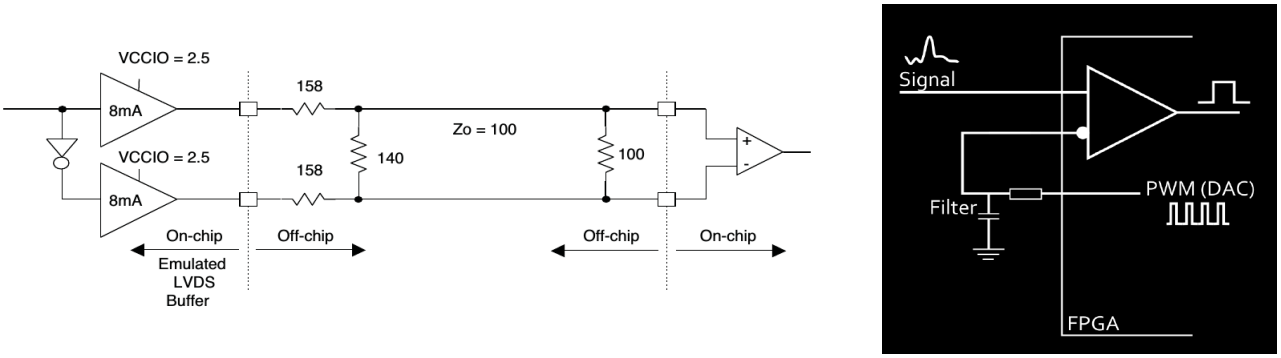


Figure 2.1: Left panel: Possible solution for a LVDS standard implementation with Lattice MachXO2 devices [35]. **Right panel:** Scheme of the signal discrimination via the LVDS input buffers. Thresholds to the input signals are set by an Digital-to-Analog-Converter (DAC) using Pulse Width Modulation (PWM) in combination with a low pass filter [36].

2.2 Time Digitization in FPGAs using the Tapped Delay Line Method

The TRB3 platform (see section 2.5 for more details) implements among others 260 high precision Time-to-Digital-Converters (TDCs) in four Lattice EPC3 FPGAs. The TDC architecture, is based on the interpolation method. A fine time measurement block, a coarse counter with granularity of 5 ns and an epoch counter is used to achieve high timing performances. The measured times are encoded and the results are converted to binary numbers. A First-In-First-Out (FIFO) memory block is used for data storage. A block diagram of the simplified TDC design is shown in Fig. 2.2 (left panel). The fine time measurement is based on the Tapped Delay Line (TDL) method [37, 38]. This method uses a delay path with well-defined delay elements, which have similar propagation delays. They are realized by using the 4-bit LUTs and the registers of the Lattice EPC3 FPGA, as delay elements and as latches respectively. The digital LVDS signals, which are generated by the FPGA discriminator (see section 2.1), are received by the FPGA LVDS input buffers. In the conventional approach the leading and trailing edges of the LVDS signal are measured using two FPGA-TDC channels. The leading edge or the trailing edge respectively is used as a start signal which propagates through the delay line. The next rising edge of the 200 MHz clock signal stops the propagation. The location of the propagating signal along the delay line defines the fine time between the start and stop signals. The time interval between different signals measured in different TDC channels can be calculated by simply taking the difference of the relevant measurement results. With this approach a time precision up to 10.2 ps between two TDC channels was achieved. A disadvantage of this approach is the higher TDC resources which are needed to measure the leading and trailing edges of a time-over-threshold signal. With a novel approach [39] it is possible to measure the time-over-threshold in a single multi-hit FPGA-TDC by using a full-asynchronous stretcher. With this approach a time precision up to 11.7 ps can be achieved in a single TDC channel. A disadvantage of this method is an extra dead time after the measurement of the trailing edge. This limits the measurement of double pulses separated in time less than the total dead time (pulse length + stretcher delay + conversion dead time). To achieve this high precision in both approaches a proper calibration has to be done. The calibration should correct the tiny delay variations in delay elements. Also temperature variations play a crucial role in an FPGA and have also be corrected via calibration.

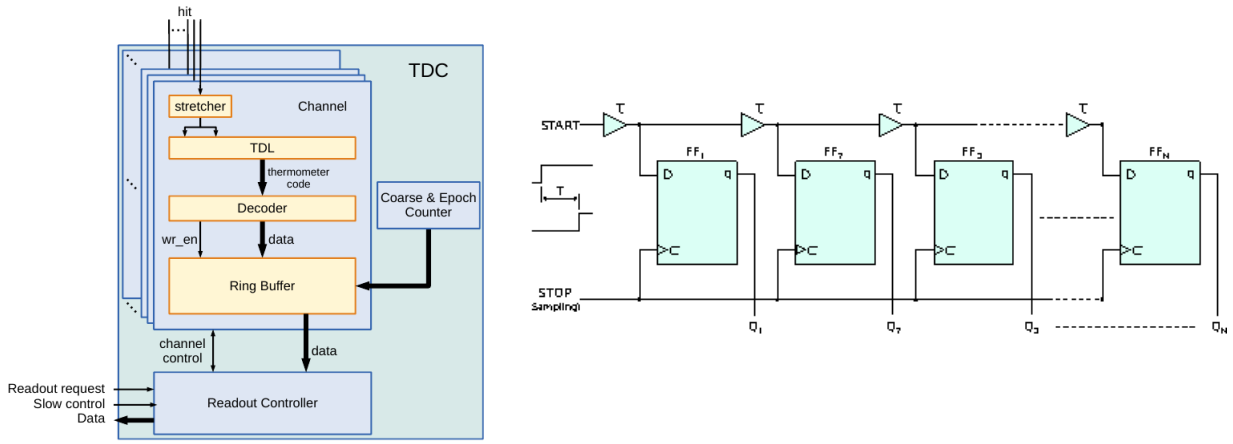


Figure 2.2: Left panel: Block diagram of the Time-to-Digital-Converter (TDC) which is implemented in an FPGA. For a precise time measurement a combination of fine, coarse and epoch time counters is used [39]. **Right panel:** The Tapped Delay Line Method (TDL) is used for fine time measurement. The rising edge of the input signal propagates through a delay line which is build out of Flip-Flops. After the next rising edge of the 200 MHz clock the propagation is stopped. The location of the propagating signal along the delay line defines the fine time [39].

2.3 The COME & KISS Charge and Time Measurement Principle

Charge information of an analog pulse can be extracted from a time-over-threshold measurement. Unfortunately this is usually not precise enough for most applications in high energy physics. A more accurate approach for a Charge-to-digital-Converter (QDC) will be introduced in the following. This method is based on a modified Wilkinson ADC [40] circuit, where the charge of an analog pulse will be encoded in the width of a digital pulse using a so called Charge-to-Time-over-Threshold (Q2ToT) or Charge-to-Width (Q2W) conversion system [34]. The simplified measurement principle is schematically shown in Fig. 2.3. The KISS (KISS concept: **K**eep **i**t **S**mall and **S**imple) part contains an attenuator/amplifier and an integration system which is made out of discrete components. The signal is split into a so called "FAST" component, containing the time information and a "SLOW" component, which is integrated by a capacitor. In order to extract the time information, the FAST signal is discriminated in a commercial (COME concept: Use **Com**mercial **E**lements) FPGA (see section 2.1). The measurement of the leading edge of the FAST signals gives the arrival time information of the analog pulse. The FPGA is also used to generate a delayed DISCHARGE signal which is used to discharge the integration capacitor. For that the FAST signal is internally delayed in the FPGA (see section 6.3.2 for more details). A logical AND gate between the leading edge of the SLOW and the delayed FAST leading edge is used to start the discharging signal with a total delay matching the input signal width. When the trailing edge of the SLOW signal reaches the threshold the discharging signal is switched off. In summary the SLOW signal is integrated by a capacitor, which is afterwards discharged linearly, through a discriminator triggered current source. Afterwards the integrated signal is also discriminated in the FPGA. The ToT of the discriminated signal, which is proportional to the charge of the input pulse, is measured in the second FPGA-TDC (see section 2.2). Consequently, three TDC channels, leading edge of the FAST and leading and trailing edge of the SLOW signal, are needed for one input channel. The analog part and the FPAG discriminator is realized on the PaDiWa-AMPS front-end board providing input to the general purpose read-out board TRB3. On this board precise FPGA-TDCs and Data Acquisition (DAQ) functionality is implemented. The two boards will be introduced in more detail in the following two sections 2.4 and 2.5.

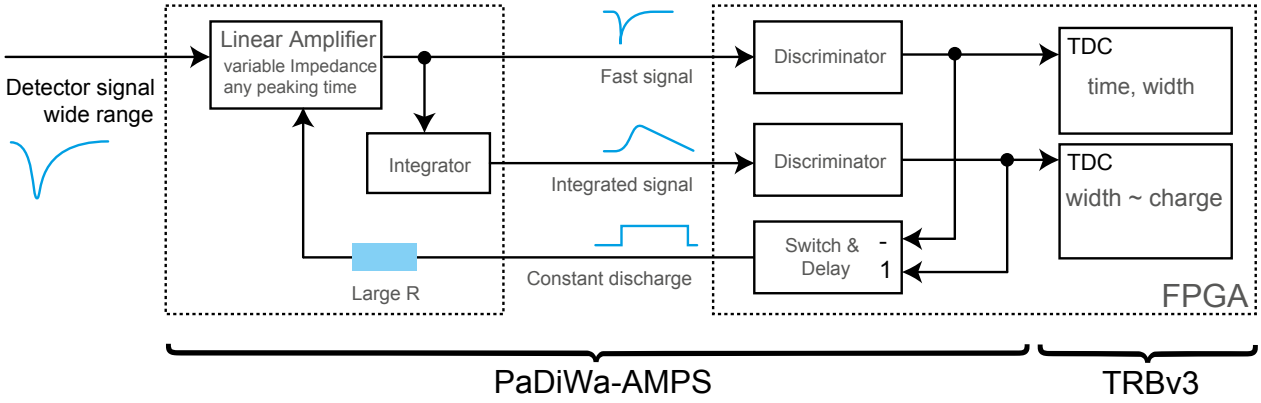


Figure 2.3: Signal chain of the COME & KISS charge and time measurement principle. The charge of an analog pulse is encoded in the width of a digital pulse using a so called Charge-to-Time-over-Threshold (Q2ToT) conversion system. After attenuation/amplification the input signal is split into a FAST component which contains the arrival time and a SLOW component which contains the charge information. The FAST signal is discriminated in an FPGA-TDC. Afterwards a FPGA TDC is used to measure its leading edge, which contains the arrival time information. The SLOW signal is integrated by a capacitor and discharged by a discriminator driven current source. Afterwards the SLOW signal is also discriminated in an FPGA-TDC.

2.4 The PaDiWa-AMPS Front-end Board for the TRB3 Platform

A first prototype board which implements the Q2ToT conversion system was manufactured at GSI. The basis of the so called PaDiWa-AMPS [34] board is the PaDiWa front-end board for the Trigger and Read-out Board version 3 (TRB3) [10]. The PaDiWa board was originally developed as a discriminator front-end board for the PANDA DIRC [41] detector. This front-end board was modified and redesigned to implement the Q2ToT measurement. In Fig. 2.4 the electronic schematic of the analog KISS (Keep it small and simple) part is shown for the first input channel. The input impedance is matched to 50 ohms. The prototype scheme has been made for pulse shapes from the HADES ECAL detector which are shown in Fig. 1.15. After the first amplification stage, using a BFS520 transistor (Q1), the signal is spit into the FAST and SLOW component. The FAST signal is sent to the FPGA for discrimination (OUTP_FAST). The SLOW part is integrated with the help of a 10 nF capacitor (C262) in a second amplification stage using the BFP740 transistor (Q2). In the FPGA a logical DISCHRAGE signal is generated (see section 6.3 for more details), which is used to discharge the integration capacitor. The SLOW signal is afterwards sent to the FPGA for discrimination (OUTP_SLOW).

Due to the simple electronic scheme, an adaption to different types of detectors is possible by changing only the values of a few resistors, capacitors and inductances. In order to adapt and optimize it to different pulse shapes (signal rise-time, width and amplitude range) the following elements (marked in Fig. 2.4) were investigated:

1. Attenuation part;
2. High frequency cut-off (low-pass filter);
3. Low frequency cut-off (high-pass filter);
4. Integrator gain.

In chapter 6 the investigations in the laboratory and the optimization process will be discussed in detail. Furthermore first steps towards an adaption and optimization of the concept for Silicon photomultipliers (Si-PM) and Diamond Detectors will be shown.

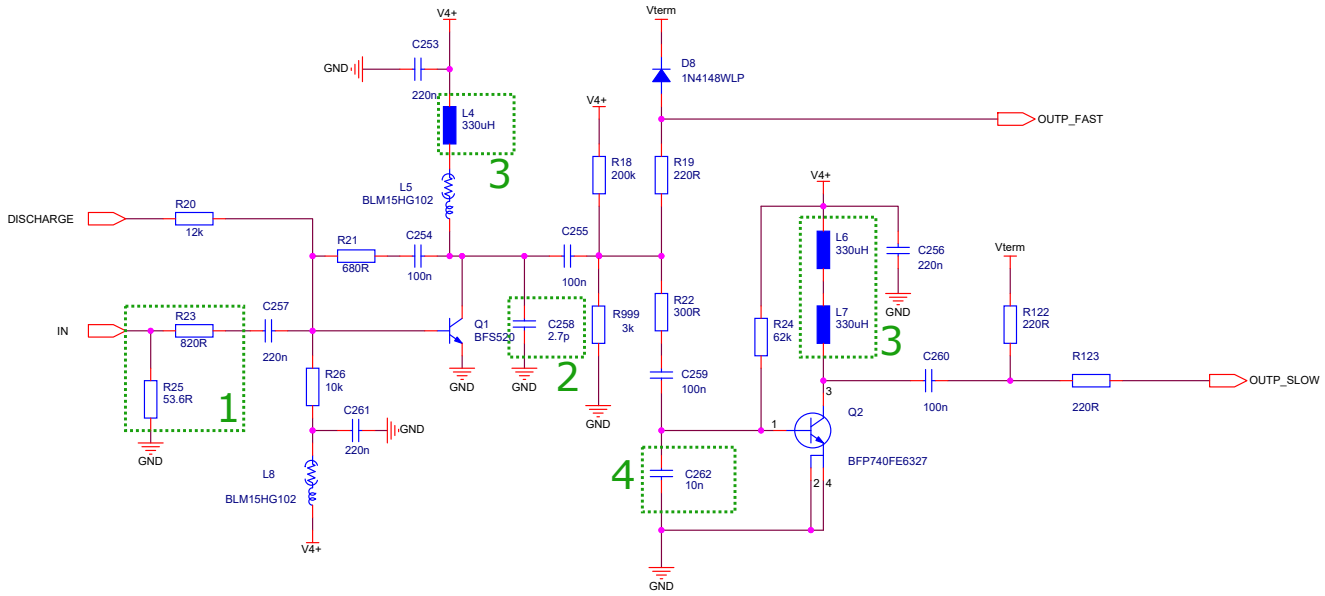


Figure 2.4: PaDiWa-AMPS electronics scheme for the first channel, excluding the FPGA. The elements which have been investigated to optimize the scheme to ECAL and other pulse shapes are labeled: 1) Attenuation part, 2) High frequency cut-off, 3) Low frequency cutt-off, 4) Integrator gain.

Several PaDiWa-AMPS prototype boards have been manufactured. The eight layer printed circuit board (PCB) has a size of 88 mm x 52 mm. The board has eight input channels which are equipped with MMCX connectors. In Fig. 2.5 a photograph and the layout of a prototype board is shown. A power supply has to provide 5 V with a current of about 800 mA. The discriminated signals are sent to the TRB3 board by LVDS via a standard 40-pole flat cable. There, the leading and trailing edges of the discriminated signals are measured. At least 24 TDC measurements are needed to measure the leading edge of the discriminated time signal and the ToT of the discriminated integrated signal. Slow control data is exchanged via a Serial Peripheral Interface (SPI) bus.

The first measurements in the laboratory have shown a time precision below 50 ps for a single channel. The relative charge resolution is below 0.5% for PMT-like pulse generator signals with an amplitude above 1 V. A dynamic range of 150 is predicted in simulations and was verified in laboratory measurements.

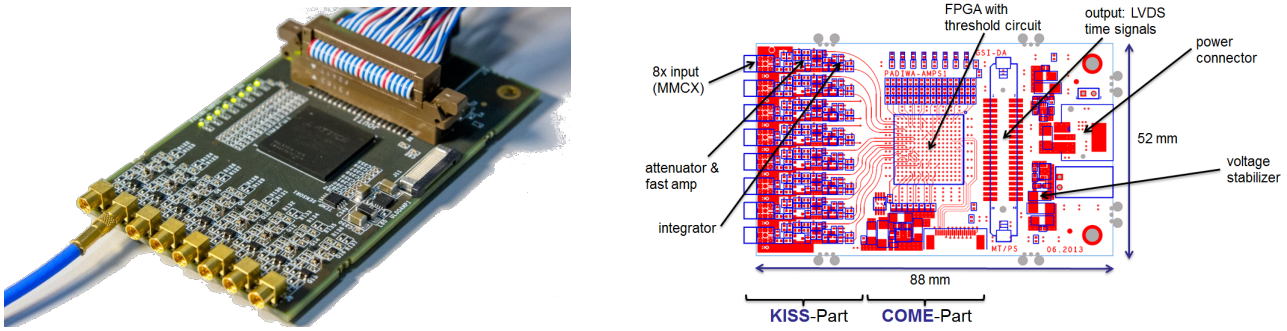


Figure 2.5: Left panel: Photograph of the first PaDiWa-AMPS front-end board prototype for the TRB3 platform. **Right panel:** Top view on the layout of PaDiWa-AMPS with some mayor parts marked. The full electronic schematics one can find in [42].

2.5 The General Purpose Trigger and Read-out Board - TRB3

The already well established general purpose read-out platform TRB3 [10, 42] is used to measure the relative time of leading and trailing edges of the PaDiWa-AMPS discriminated FAST and SLOW signals. The TRB3 platform was primordially developed for the HADES experiment. Due to its general purpose platform it attracted other experiments. The modular structure of the TRB3 allows to equip it with a lot of add-on boards. Front-end boards for different applications are available. The tapped delay line method, which was introduced in section 2.2, is used to implement up to 260 TDC channels in four peripheral Lattice EPC3 FPGAs. The board allows single edge and time-over-threshold (ToT) measurements, by using the TDC channels in pairs, with a time precision <20 ps RMS between two channels. The TRB3 can also serve as a data acquisition (DAQ) system which is controlled by a fifth central FPGA. It is equipped with an internal trigger system and the front-end electronics thresholds can be set through slow control lines. In table 2.1 the key facts of the TRB3 board are summarized. The board is applicable as a standalone system and also in large systems with many TRB3 boards. The data is sent through gigabit Ethernet to a personal computer on which they are saved in so called Hades List-mode Data (HLD) files. Those files can be unpacked using a suitable software and then analyzed with the help of the ROOT Data Analysis Framework [43]. Furthermore, the DAQ framework DABC (Data Acquisition Backbone Core) [44] in combination with the GSI Object Oriented On-line Off-line system (Go4) [45] analysis tool can be used as an alternative for analysis and online monitoring of the data. A detailed description of the software and read-out packages will be given in section 2.6.

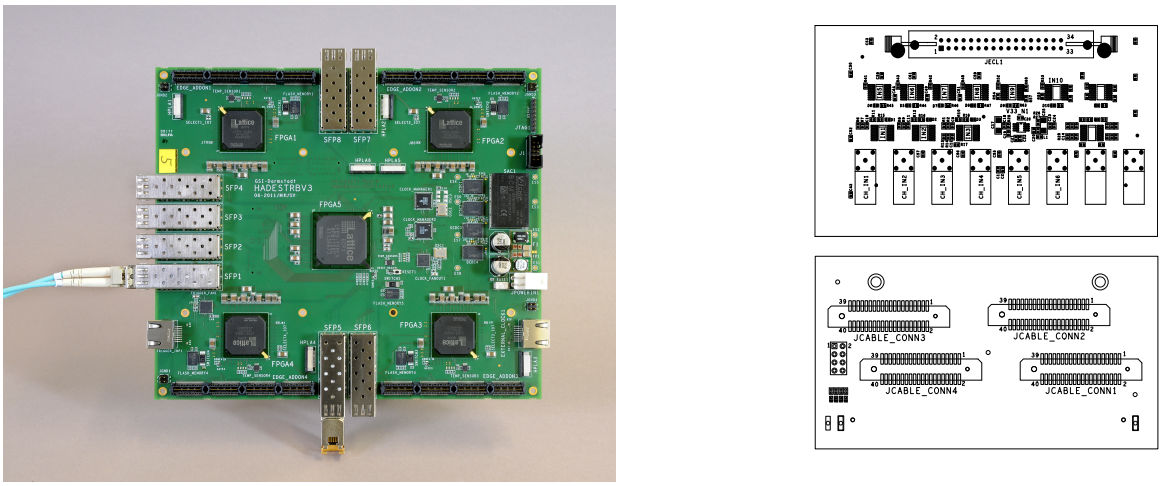


Figure 2.6: Left panel: Photography of the TRB3 board which is equipped with five FPGAs. In the central one the data acquisition and trigger system is implemented. In the four outer FPGAs 260 TDC channels are implemented. They are used to measure the ToT of the FAST and SLOW signals, which are discriminated by the PaDiWa-AMPS front-end board (Photography by Gaby Otto, GSI). **Right panel:** It is possible to extend the TRB3 platform with several add-on boards. During this work the 4conn AddOn (upper layout) and the GPin AddOn (lower layout) have been used [42].

Key	Facts
Supply Voltage	48 V (40-50V), galvanically isolated on board
Power Supply Current	0.5A minimum without AddOns
GbE-connectivity	max. 95 MBytes/s transfer per link
GbE-slow-control	up to 400 registers/transfer, speed depends on GbE latency
Connectivity	Max. 8 SFPs, each 2GBit/s on board. 4 AddON boards
Max Readout Trigger Rate	about 300 KHz
Max Hit Rate	50 MHz (burst of 63 hits)
TDC Channels	260 (Single edge detection)
Time Precision	<20 ps
Minimum pulse width	<500 ps

Table 2.1: Summary of some key facts of the TRB3 platform [42].

2.6 The Control and Read-out Software Packages

The TRB3 is already in use by the HADES experiment, therefore its firmware is fully compatible with the TrbNet network. The general HADES TrbNet scheme was already introduced in section 1.2. The custom network consists out of three channels, which are used for triggering, data transport and slow control. One channel is blocked by the Central Trigger System (CTS) [46], which generates the trigger information and initiates the TRB3 boards to send their data. The CTS is implemented in its central FPGA. A wide spectrum of functionality is available, such as random pulsers and coincidence detection. A self-triggering mode or external triggers can be used. The implementation allows the extension via modules. The CTS can be operated in a triggering master or slave mode. For slow control another channel is blocked in the TrbNet.

The by the CTS requested data is send to the event builders using another TrbNet channel. The well established HADES event-builder software [47] can be used to acquire the data which is delivered by the front-end. The data is stored on hard disks in the so called HADES List-mode Data (HLD) files. The TDC data can be analyzed and calibrated offline by an unpacker code which is based on the ROOT Data Analysis Framework [43]. As an alternative, the DAQ framework DABC (Data Acquisition Backbone Core) [48, 44] in combination with the GSI Object Oriented On-line Off-line system (Go4) [48, 45] analysis tool can be used for analysis and live monitoring. The read-out structure is shown in Fig. 2.7. The data from the TRB3 is send via the UDP protocol to the DABC server. It is possible to use an automatic TDC calibration which is calculated from the received TDC data itself. The data from other TRB3 board are combined in a so called Combiner and afterwards saved to HLD files on the disk. It is possible to run Go4 analysis software via a TCP/IP socket connection in parallel. This allows to visualize the received data in real-time on the Go4 GUI. In Fig. 2.8 a screen-shot of a running analysis is shown. An lightweight HTML based Web control interface can be used to start the readout process and visualize analysis results.

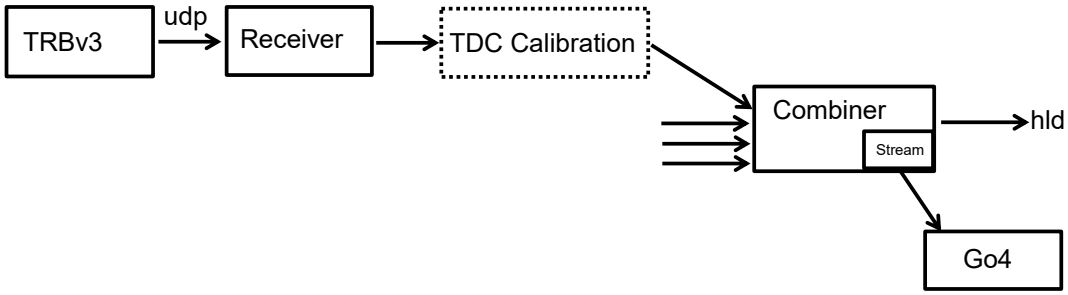


Figure 2.7: DABC and Go4 read-out scheme showing the data transport from the TRB3 board. An automatic TDC calibration can be performed in real time. It is also possible to calibrate the TDCs with calibration data generated from the hld file. This is useful for important data, because the automatic calibration can not be undone.

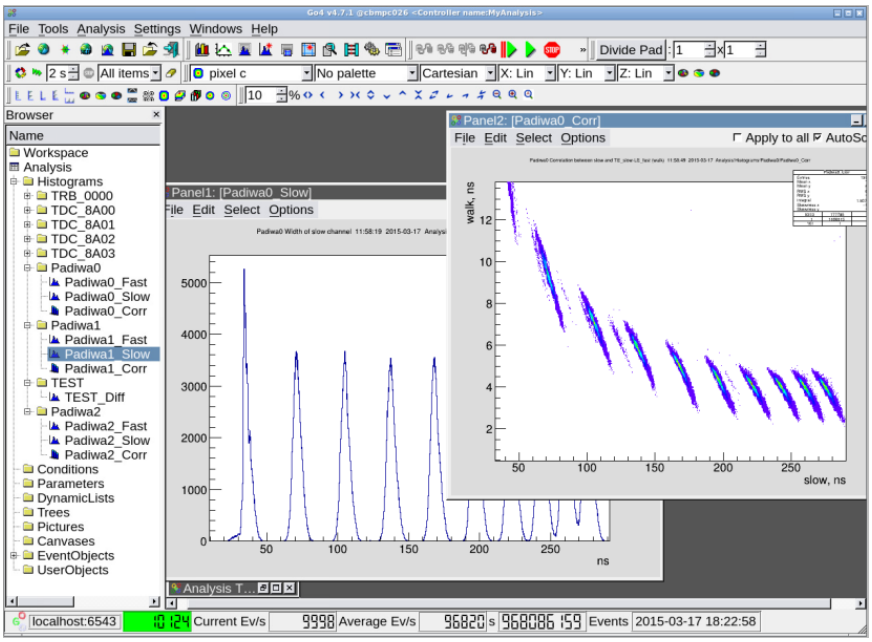


Figure 2.8: Screen-shot of the Go4 GUI. A ROOT based analysis can be displayed in real-time.

3 Characterization of the PaDiWa-AMPS Prototype for ECAL PMT Read-out

The first version of the PaDiWa-AMPS board has been developed for the HADES ECAL detector, which is being built. Several prototype boards have been manufactured at GSI. In this chapter the characterization of the first prototype boards for PMT read-out will be discussed. For that a full TRB3 read-out chain was set up in the laboratory. The Q2ToT read-out concept was studied with pulse generators and with ECAL modules. Laboratory tests have been done to characterize the front-end board in regarding time precision, charge precision, dynamic range and rate capability. In this chapter the laboratory set-up will be introduced. By means of typical analog signals from the analog part of the PaDiWa-AMPS board, the threshold settings will be explained. The results will be shown in the following.

3.1 The Laboratory Set-up

A set-up for the characterization of the PaDiWa-AMPS prototype board is located in the Detector Laboratory (DL) of GSI. There, the full TRB3 based read-out system has been set up. In Fig. 3.1 a photography of the set-up is shown. The PaDiWa-AMPS prototype board is connected to a TRB3 via a 1 m long 40-pol LVDS flat cable. The TRB3 board is connected to a personal computer via Ethernet. The DABC+Go4 software packages, which have been introduced in section 2.6, are used for the data processing. With this software it is possible to run ROOT analysis macros in real-time, which is very useful in laboratory test. The PaDiWa-AMPS front-end is powered by a Hameg HMP4040 switching power supply, which provides the needed supply voltage of 5 V. The TRB3 board is powered with a GW Instek PSP 405 power supply, which provides the needed supply voltage of 40 V. Test pulses can be generated by pulse generators (in short: pulsers). For that a Tektronix AFG3252 and an Agilent 33220A pulsers are available. In addition, a battery powered pocket pulser can be used. Besides pulsers several HADES ECAL modules, equipped with different types of PMTs, are available. Signals can be generated by illuminating the lead glass with LED light. Signals from cosmic muons can be selected by requiring a coincidence of two plastic scintillators. The trigger, which starts the read-out process of the TRB3 board, is realized in two ways. On the one hand the TRB3 can operate in a self-triggering mode, were it can trigger on the input signals itself. On the other hand it is possible to use an external NIM trigger signal, i.e. from a pulse generator. Due to the fact that pulsers normally provide a TTL synchronization signal, the signal has to be converted into a NIM signal. This can be done with the help of a LEVCON1 Converter-Module (developed at GSI). Subsequently the NIM signals can be send to the GPin AddOn [42] for the TRB3 were leading and trailing edges are measured and can be used as a trigger. For investigations of the PaDiWa-AMPS analog part a R&S® RTO1044 20 GS/s digital oscilloscope was used. Signals can be probed with standard single-ended and R&S® RT-ZD40 active differential probes.

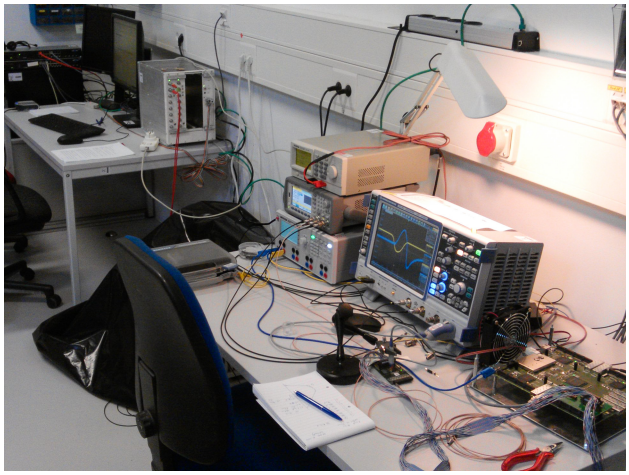


Figure 3.1: Set-up for the characterization of the PaDiWa-AMPS prototype board, located in the Detector Laboratory (DL) of GSI. The PaDiWa-AMPS board is connected to a TRB3, which is connected to personal computer via Ethernet. Test signals generated by laboratory pulse generators and ECAL modules can be used to test the performance of front-end broad.

3.2 Analog Signals and Threshold Settings

The input signals, generated by pulsers, have been chosen to be similar to ECAL PMT pulses. Therefore triangular shaped pulses with a rise time of 2.5 ns (10%, 90%) and a fall time of 50 ns (10%, 90%) are used. Pulses are generated by varying the amplitude, keeping the time parameters constant. This emulates an ECAL response of different measured energies (see Fig. 1.15). The screen-shot from a digital oscilloscope in Fig.3.2 shows typical signals from the analog part of the PaDiWa-AMPS board. Single ended probes have been used to investigate the analog signals. Besides the input signal (split in front of the input), the FAST (measured at R19, see Fig. 2.4), the SLOW (measured at R123, see Fig. 2.4) and the DISCHARGE (measured at R20, see Fig. 2.4) signals are shown.

Figure 3.2: Scope picture showing some characteristic analog signals, probed on the PaDiWa-AMPS board. The yellow signal shows the input signal which was generated by a pulser. The blue signal shows the FAST signal (measured over R19). The DISCHARGE signal (measured over R20) is shown in green. The SLOW signal (measured over R123) is shown in magenta. Signal reflections are mainly introduced by the probe. Taken from [49].

The discriminator and threshold setting mechanism of the PaDiWa-AMPS board has been already introduced in section 2.1. The LVDS input buffers of the FPGA are used as a comparator. The thresholds voltages are set by a DAC which consists of a PWM inside the FPGA and a low pass filter circuit outside the FPGA. A 16-bit register is reserved for threshold values. This allows the setting of threshold voltages from 0 mV up to the reference voltage of 3300 mV in steps of 0.5 mV. In Fig. 3.3 (left panel) the linearity between the set thresholds and measured threshold voltages on the board is shown. In Fig. 3.2 (right panel) the signal polarity of the FAST and the SLOW signals are schematically shown. The FAST output signals have a positive polarity (see Fig. 3.2) and the baseline is located at around 60 mV. The SLOW signals have a negative polarity (see Fig. 3.2) and the baseline is located at around 2890 mV. This information is important for a proper setting of the thresholds. In Fig. 3.3 (right panel) the deviation of the set threshold and the measured threshold voltage on the board is shown for FAST and SLOW channels. The measured FAST threshold voltages differs less than 0.6 mV from the set value of 100 mV. The measured SLOW threshold voltages shows an offset of about 25 mV from the set value of 2850.3 mV, but the deviation around the offset is below 2 mV. A hysteresis free threshold setting behavior was observed in the laboratory. The FPGA discriminator is also free of hysteresis. With help of the threshold and the TDC count rate, which is displayed in the CTS GUI, the width of the baseline was analyzed. The width is correlated with the amplitude of the noise in the corresponding channel. The result for a SLOW channel is shown in Fig. 3.4 (right panel). A width of about 7 mV has been determined. The flat top of the distribution can be explained by exceeding the maximum rate capability of the FPGA-TDCs in the TRB3, which is at around 35 MHz. These measured widths are in agreement with measurements performed using the oscilloscope.

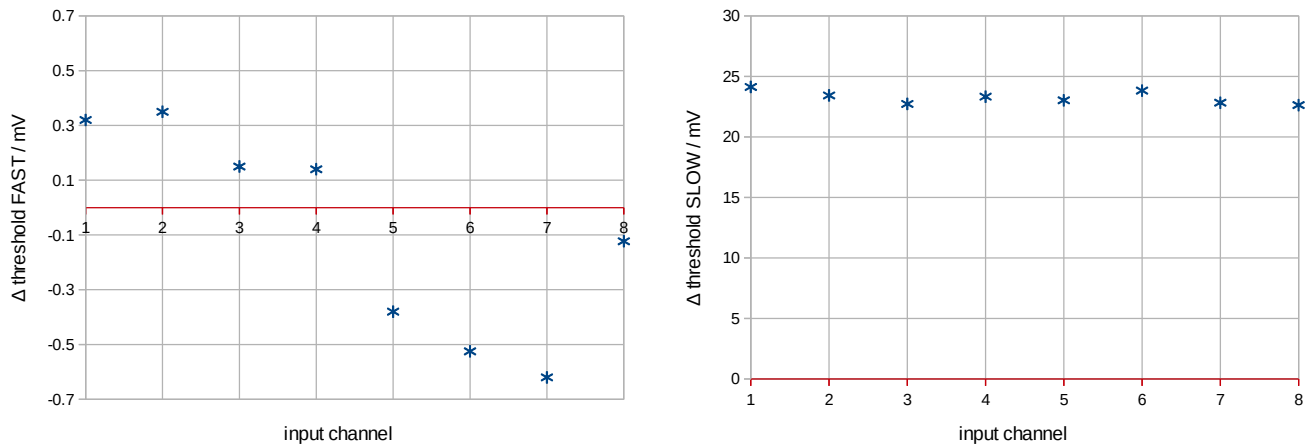


Figure 3.3: Deviations of measured threshold voltages on the board for a fixed set threshold in the PaDiWa-AMPS control GUI. The FAST channels (left panel) were set to 100 mV. The maximum deviation is about 0.6 mV. The SLOW channels (right panel) were set to 2850.3 mV. An offset of about 25 mV is observed, but the deviation around the offset is below 2 mV.

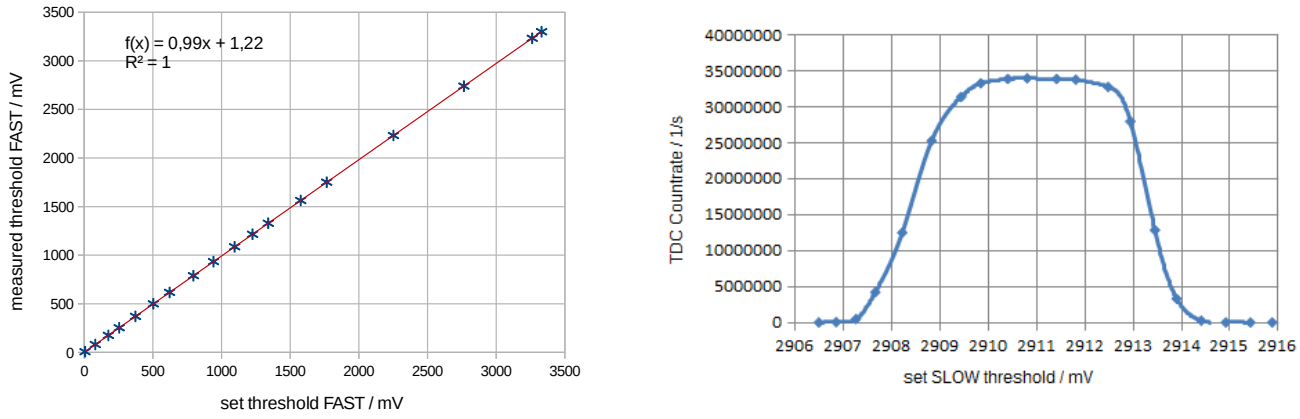


Figure 3.4: Left panel: The measured threshold on the board shows a linear behavior with a small offset to the threshold set in the GUI. **Right panel:** The TDC count rate (obtained from the CTS GUI) as a function of the set threshold for a SLOW channel. The flat top of the distribution is due to the FPGA-TDC counting rate limitation of the TRB3 board.

3.3 Time Precision Measurements

An important performance parameter of the PaDiWa-AMPS front-end board is its time precision. It is usually characterized by the width of the distribution of a repeated time measurement. In the following the sigma of a fitted Gaussian distribution is used for characterization. The FAST channel is designed for the timing measurements and the arrival time information is encoded in its leading edge. The time precision of the PaDiWa-AMPS board was investigated using two approaches which are schematically shown in Fig. 3.5 (left panel).

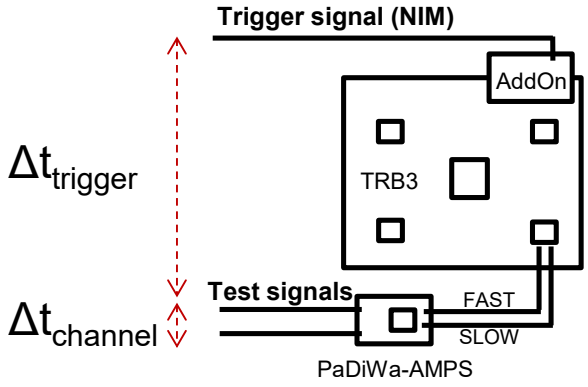


Figure 3.5: Laboratory set-up for the characterization of the time resolution.

In the first analysis the time precision between two input channels was determined. For that a test signal from a pulser was split and sent into two neighbored PaDiWa-AMPS input channels. In each channel the leading edges (t_1 and t_2) of the FAST signal are measured. The time difference between both leading edges, shown in Fig. 3.6 (left panel), has been fitted with a Gaussian. From this a time precision of $\sigma_{t_1-t_2} = 27\,\text{ps}$ could be determined between two channels. By assuming that both channels have the same contribution to the measured time precision, for a single channel a time precision of $\sigma_{t_1} = \sigma_{t_2} = \frac{\sigma_{t_1-t_2}}{\sqrt{2}} = \frac{27\,\text{ps}}{\sqrt{2}} = 19\,\text{ps}$ can be calculated.

In a second analysis the time precision relative to an external trigger was determined. For that a pulser signal was split into two signals. The first signal is sent directly to the PaDiWa-AMPS board. The second one is converted into NIM and used as an external trigger signal for the TRB3. The time differences between both signals is shown in Fig. 3.6 (right panel). The obtained time precision is $\sigma_{t_1-t_{trigger}} = 83\,\text{ps}$.

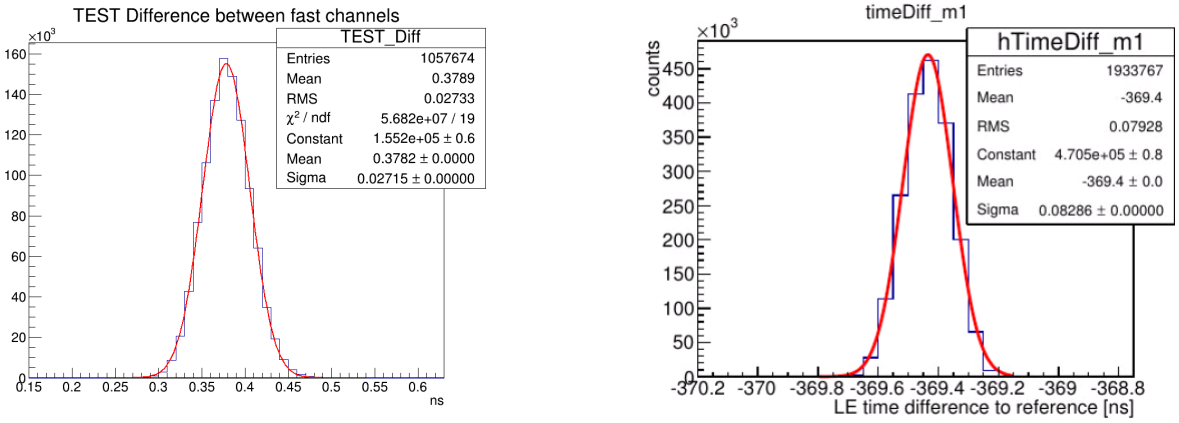


Figure 3.6: Left panel: Time difference between two channels by splitting the input signal. A time precision of $\frac{\sigma_{t_1}}{\sqrt{2}} = 19\,\text{ps}$ was determined for a single channel. **Right panel:** Time difference relative to the trigger signal. A time precision of $\sigma_{t_1 - t_{trigger}} = 83\,\text{ps}$ was determined.

3.4 Charge Resolution and Dynamic Range

The measured charge depends on the width and the amplitude of the input pulse. The charge measurement of a pulse is converted into a width measurement, which is encoded in the width of the SLOW signal. In an naive way one can calculate the charge from the SLOW signal only, using the following expression:

$$\text{charge} \propto \text{Q2ToT}_{\text{naive}} = \text{TE}_{\text{SLOW}} - \text{LE}_{\text{SLOW}}. \tag{3.1}$$

Here the abbreviations for the leading (LE) and the trailing (TE) edge of the SLOW signals are used. From measurements in the laboratory it was found that a better way to determine the charge, with a higher precision, is to use the trailing edge of the SLOW and the leading edge of the FAST signal:

$$\text{charge} \propto \text{Q2ToT}_{\text{better}} = \text{TE}_{\text{SLOW}} - \text{LE}_{\text{FAST}} \tag{3.2}$$

This improves the charge resolution because of a jitter observed in TE_{SLOW} signals. The LE_{FAST} shows less jitter. In the following the second definition 3.2 is used for the width determination of the SLOW signal which represents the charge. In Fig. 3.8 (left panel) the charge measurement for different pulses is shown. Triangular shaped pulses (rise time: 2.4 ns, fall time: 50 ns) were generated by a pulser. Their amplitude was varied and the $\text{Q2ToT}_{\text{better}}$ was measured. Afterwards the distributions have been fitted by Gaussian functions. The fitting parameter for mean and sigma are used to characterize the charge and its resolution which is defined in the following by

$$\text{charge resolution} = \frac{\sigma}{\text{mean}} \cdot 100\%. \tag{3.3}$$

The charge resolution as a function of the signal amplitude is shown in Fig. 3.7. For input amplitudes lager than 3.5 V the resolution is below 0.5%. It should be noted that the pulser itself introduced noise which dominated the measurement resolution.

A time walk effect is present in every threshold triggered discriminator. It causes a dependence of the trigger time on the amplitude of the signal. This effect dominates especially for signals with small amplitudes and deteriorates their charge resolution due to low frequency base line shifts (low frequency noise). An offline walk correction can be applied to correct the jitter of the measurement $\text{Q2ToT}_{\text{better}}$ by using the jitter between the leading edges of the FAST and SLOW signals. The walk is defined by

$$\text{walk} = \text{LE}_{\text{SLOW}} - \text{LE}_{\text{FAST}}. \tag{3.4}$$

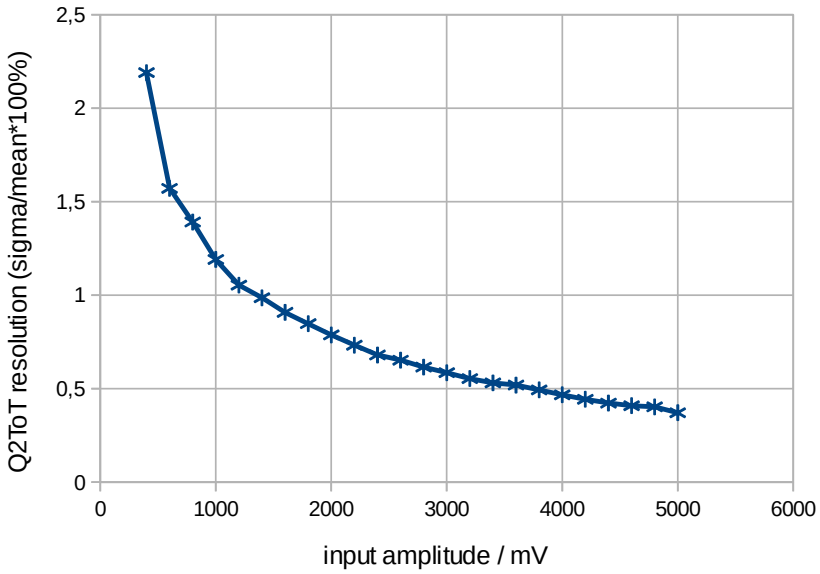


Figure 3.7: Relative charge resolution, which is defined by sigma/mean*100 [%], for different input amplitudes. Signals with variable amplitude from a laboratory pulses with similar shape as HADES ECAL pulses have been used. For signals amplitudes above 1.5 V the resolution is below 1%.

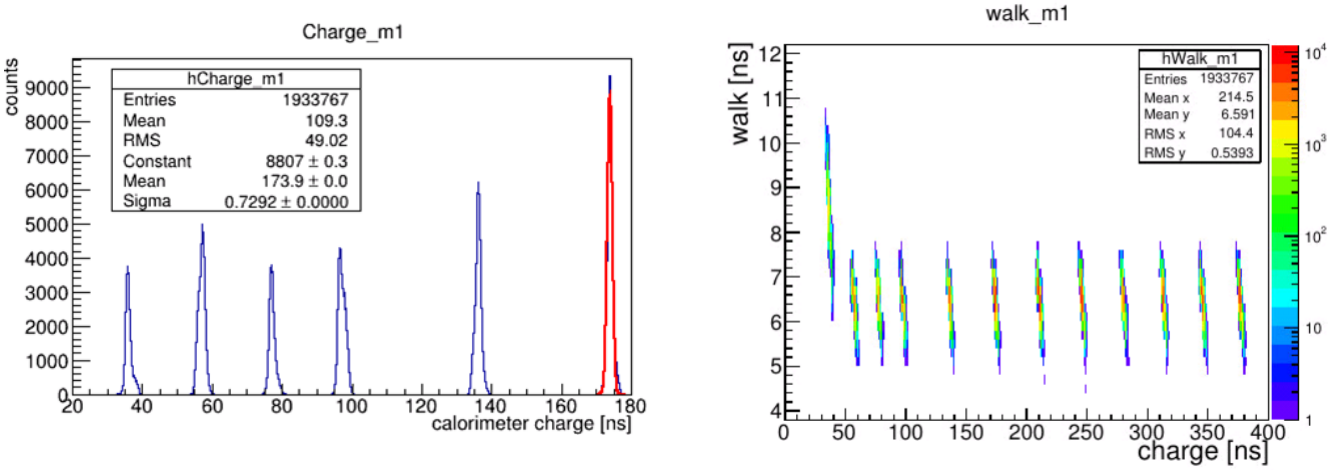


Figure 3.8: Left panel: Typical result from a charge measurement. The amplitude of the input pulse was varied while holding the width of the pulse constant. Here the width of the SLOW signal is defined by trailing edge of SLOW minus leading edge of FAST. After fitting with a Gaussian the mean and sigma is used for the characterization. **Right panel:** Walk effect which can be corrected offline to improve the charge resolution especially for small signal amplitudes.

In the two dimensional histogram in Fig. 3.8 (right panel) the walk effect is shown for different measured charges. A walk correction can improve the charge resolution especially for small signals.

The dynamic range is another important property of the read-out electronic. It is defined by the ratio between the largest and smallest measurable signal amplitude. The dynamic range of the PaDiWa-AMPS front-end has been studied in the laboratory. For that a scan with different input amplitudes was done. To achieve the highest possible dynamic range the threshold settings are important. It has been found that the FAST threshold should be very close to baseline to achieve the best time resolution. The SLOW threshold is more challenging due to the high sensitivity to low frequency noise. Here also a threshold

setting as close as possible to the baseline is an effort. The dynamic range of the first version of PaDiWa-AMPS is shown in Fig. 3.9. The FAST channel saturates quite early. The SLOW channel shows a linear behavior with only small saturation effects. With a perfect threshold setting a dynamic range of about 150 can be covered. It is difficult to measure the charge of signals with amplitudes below 40 mV using the proposed concept. This is due to noise in the SLOW channels which make a very low threshold setting impossible. Large efforts were made to reduce the noise in order to increase the dynamic range (see section 6.2).

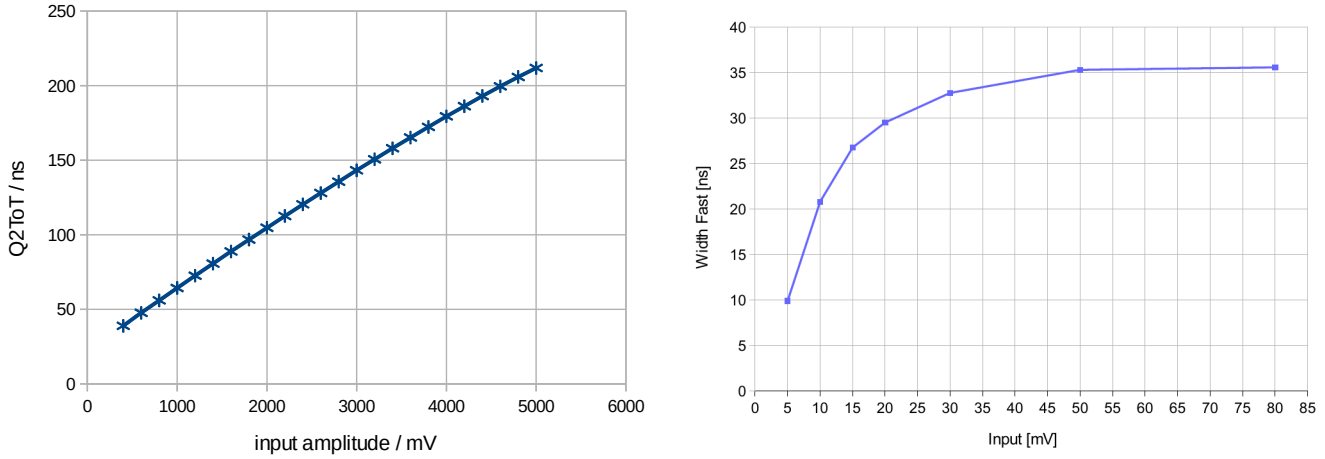


Figure 3.9: Left panel: Dynamic range of the SLOW signal width (Q2ToT) for the first PaDiWa-AMPS prototype which is not fully optimized for ECAL pulses. The dynamic range is about 150. The trend is in the beginning quite linear, at higher higher input amplitudes saturation results in small bending of the width. The smallest amplitude which can be measured is about 40 mV **Right panel:** Dynamic range of the FAST signal width. This channel is quite sensitive, pulse amplitudes starting with 10 mV can be measured. A saturation of the width starts quite early.

3.5 Estimation of the Rate Capability

The rate capability of the front-end electronic is also an important quality. In Fig. 3.10 the measured Q2ToT is shown as a function of the signal frequency. The charge is constant up to about 100 kHz, were the measured charges start to decrease. This effect can be explained by an overshoot which is observed in the SLOW signal (see Fig. 3.11) The natural decay of the overshoot is in the order of μs. With sufficient high pulse rate the SLOW signal is influenced by the overshoot from the previous pulse. Consequently a smaller width is measured because of the fixed threshold voltage. In section 6.2.4 it will be shown that the over shoot could be slightly reduced and therefore the rate capability could be increased. Only an active baseline restorer will be able to reduce this effect dramatically.

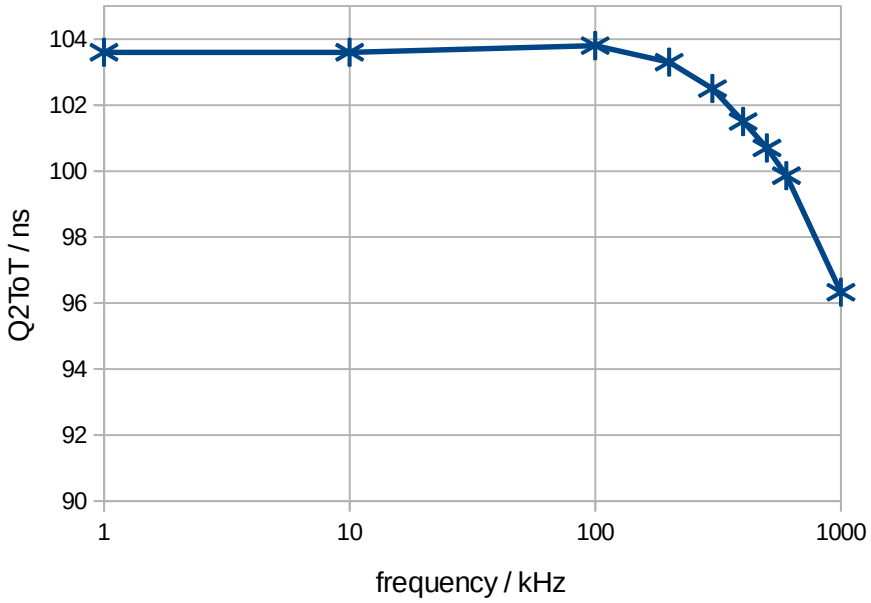


Figure 3.10: Rate capability for the first prototype. For rates above 100 kHz the measured Q2ToT decreases.

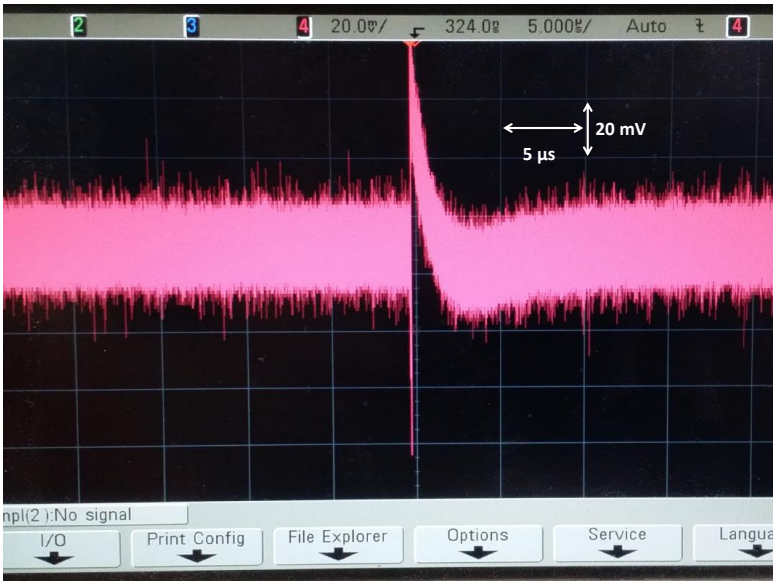


Figure 3.11: The rate capability is limited by an overshoot in the SLOW signal which has a natural decay time in the order several μs.

4 HADES ECAL Test Beam-time with secondary Photon Beam at the MAMI Facility

In January 2014 a test beam-time with secondary photon beam was successfully performed at the MAMI (Mainz Microtron) facility of Johannes Gutenberg-Universität Mainz. Tests with HADES ECAL modules [50] were motivated by the following two major points. The first point was the characterization of the performance and the energy resolution of the lead glass modules equipped with three different types of PMTs. The second point was the characterization of the read-out electronics. Two systems have been systematically studied. The first one is the pulse shaping front-end board developed in Cracow [51] in combination with the SHOWER-AddOn ADC for the TRB2 platform and the second one is the PaDiWa-AMPS front-end board for the TRB3 platform. Reference measurements were performed with a commercial CAEN DT5742 12 bit 5 GS/s Waveform Digitizer in combination with the GSI MA8000 (developed at GSI) main amplifier and shaper but also by a R&S® RTO1044 20 GS/s oscilloscope. In the following an overview of the experimental setup is given. The measured energy resolution by the PaDiWa-AMPS is shown for different ECAL modules and the results are compared with the reference electronic.

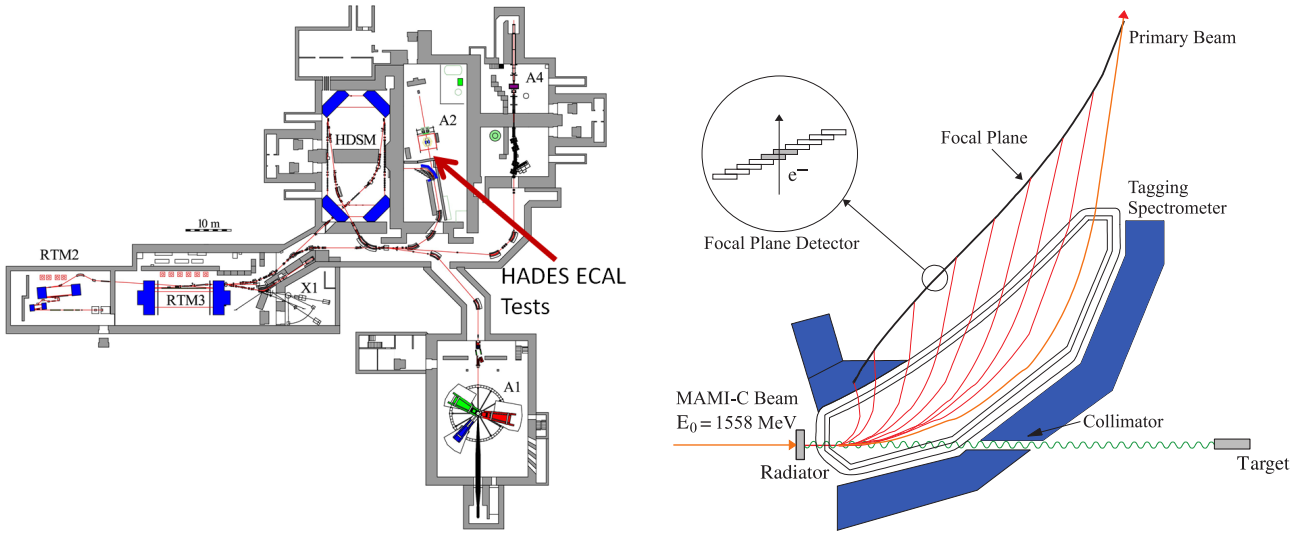


Figure 4.1: Schematic picture of the MAMI facility in Mainz (left panel). The HADES ECAL tests took place in front of the Crystal Ball Experiment which is located in area A2. After acceleration of the electrons, in four microtron stages, the secondary photon beam is generated by a copper radiator in front of the tagger spectrometer (right panel) [52]. The tagger spectrometer provides triggers which allow the selection of gammas with energies between 80 and 1400 MeV. The ECAL modules (indicated as Target on the right figure) were placed behind the beam collimator [53].

4.1 Experimental Set-up and the Trigger Generation

In Fig. 4.1 (left panel) the MAMI facility in Mainz is shown. The accelerator complex consists of four microtron stages which allow an acceleration of electrons up to energies of $E_e = 1.6$ GeV. Beam current

up to 100μA can be achieved. The HADES ECAL tests took place in the hall A2. The set-up was located between the exit window of the tagger spectrometer and the Crystal Ball experiment.

Electrons with an energy of $E_e = 1558$ MeV are impinge on a copper radiator with a thickness of 10 μm to produce gamma rays via Bremsstrahlung process. Due to a magnetic field with a field strength of 1.83 T inside the Tagging spectrometer (Tagger), the electrons are deflected towards a focal plane detector. The deflection angle is proportional to the energy of the electrons and therefore also to the energy of the gamma rays. Each focal plane of the detector is assigned to a Tagger channel number. A logical AND between the tagger channels and a master trigger allows the selection of the energy of the gamma rays. The Tagger has in total 352 detector channels which allow a selection of energies from E_γ=1401 MeV down to E_γ=81 MeV. For the ECAL test eight channels were selected. In table 4.1 the selected tagger channels and their corresponding gamma energies are shown.

Tagger channel	E_γ (mean) in MeV	E_γ (width) in MeV
2	1399.3	2.0
66	1217.8	3.3
121	1032.4	4.0
170	843.4	4.3
210	678.1	4.7
261	461.3	4.8
306	270.9	4.9
352	81.4	4.8

Table 4.1: List of selected Tagger channels and their corresponding gamma energies and their widths [50].

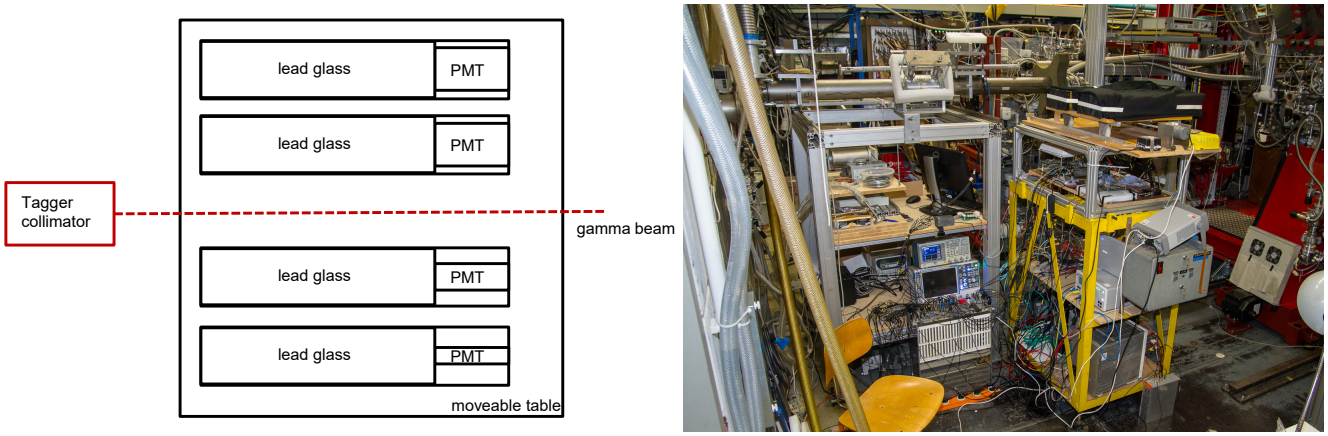


Figure 4.2: Left panel: Schematic top view of the movable platform, equipped with four ECAL modules. The front plate of the modules were located 1 m downstream of the tagger exit window (marked as a red box). **Right panel:** Photography of the ECAL test set-up. The movable table equipped with the ECAL modules is placed on a yellow support frame. Beam direction is from left to the right side. Trigger and read-out electronics are placed under the movable platform and in a second shelf.

Four ECAL modules were placed on a movable platform about 1 m downstream of the tagger exit window. The photon beam was shaped using a collimator with a diameter of 2 mm, placed at the exit window of the Tagger. This results in a beam spot with a diameter of about 6 mm at the front plate of the ECAL module. The movable platform allowed the test of different ECAL modules during a beam run without entering the experimental hall. In Fig. 4.2 a schematic picture and a photography of the setup

are shown. Three types of PMTs have been intensively tested and compared. In table 4.2 the used ECAL modules, their operation high voltage (HV) and their position on the movable platform are shown.

Module name	PMT type	Operation HV in V	Table position
8	EMI 9903KB (1.5")	1400	1
VH3	Hamamatsu R6091 (3")	1650	2
VH6	Hamamatsu R6091 (3")	1750	4
MH5	Hamamatsu R8619 (1")	1300	5

Table 4.2: List of used ECAL modules. The photomultiplier type, the operation voltage and the position on the movable platform are listed.

In Fig. 4.3 (left panel) a schematic picture of the PaDiWa-AMPS and TRB3 read-out set-up, as it was used during the beam time, is shown. The ECAL modules have been connected to a PaDiWa-AMPS board via standard 50 ohms LEMO cables. Three different trigger signals were generated and fed to a TRB3 GPin AddOn. The Master Trigger, which was provided by the Tagger, was sent to the first channel. The eight chosen photon energies were separated by dedicated trigger logic. For that each of the eight Tagger triggers, which correspond to different photon energies, were equipped with different cable delays. A logical OR between the eight delayed Tagger triggers generated the final trigger for the TRB3 which was sent to the second channel of the GPin AddOn. In Fig. 4.3 (right panel) the trigger counts over the time is shown for a beam run. Each peak corresponds to one of the eight selected photon energies. In the analysis a time window can be set on a peak to select only the hits with the corresponding energy. A third trigger signal was generated by an additional plastic scintillator which was placed behind a tagger channel. Its trigger signal is not affected by the Tagger trigger electronics provided by the MAMI accelerator and was used to study the time resolution of the ECAL modules. During the experiment the total load on the detector was around 5 MHz. The read-out process was triggered with a frequency of about 100 Hz.

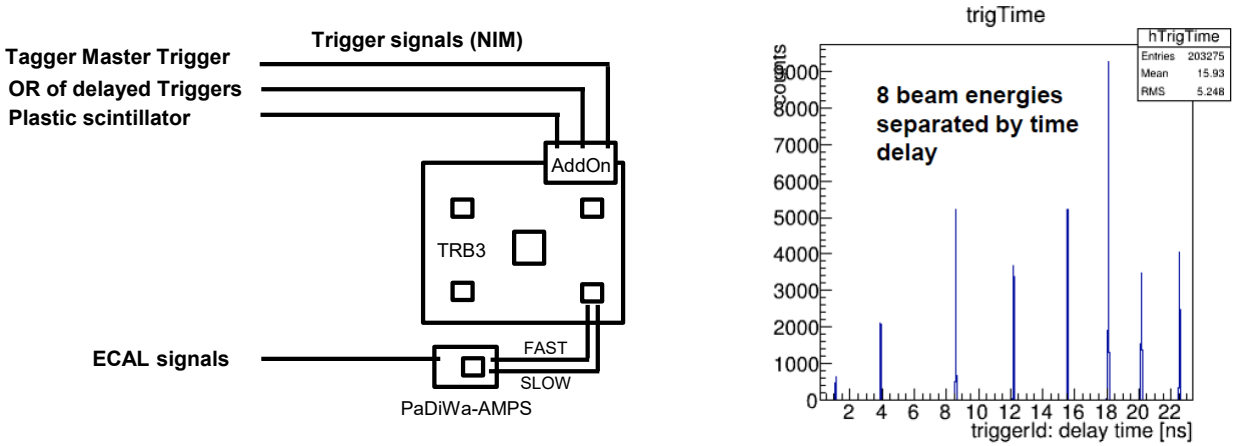


Figure 4.3: Left panel: Schematic picture of the PaDiWa-AMPS readout scheme. The ECAL modules were connected to the PaDiWa-AMPS front-end board which is connected to the TRBv3. Master Trigger, delayed trigger OR and discriminated signal of the additional plastic scintillator were connected to a GPin AddOn board. **Right panel:** The eight gamma energies were separated by generating a logical OR with the different delays (right panel).

4.2 PaDiWa-AMPS Measurement Results

In this section the calibration process and the determination of the energy and time resolution of the system, which could be achieved with the PaDiWa-AMPS front-end board is shown. The obtained results are compared with the Cracow ADC + TRB2 electronics and the reference CAEN flash ADC measurement.

4.2.1 Calibration and Determination of the Energy Resolution of ECAL Modules

For the calibration process the Q2ToT was calculated for each energy. The Q2ToT distributions were fitted by Gaussian functions from which the mean (μ) and sigma (σ) values were extracted. Fig. 4.4 shows the calibration curves for all three PMT types. The mean value of the Q2ToT measurement is plotted as a function of the beam energy. The 3 and 1.5 inch PMT ECAL modules showed a linear behavior. For the module equipped with a 1 inch PMT a saturation effect could be clearly observed. This effect was already observed in the laboratory test measurements. The reason of this non-linearity is due to the operation of the PMT at high voltages which was close to the maximum operating voltage recommended by the manufacturer.

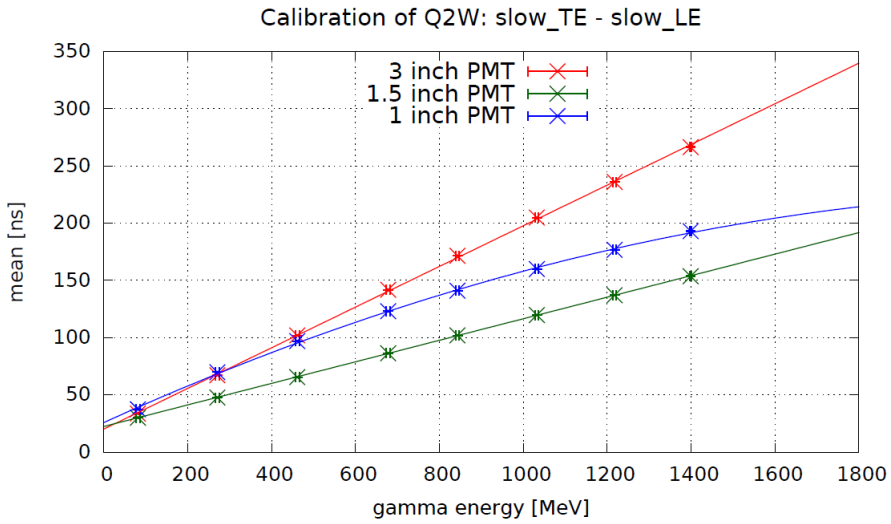


Figure 4.4: The calibration curves for 3 and 1.5 inch PMT modules show a linear behavior. The module equipped with a 1 inch shows a saturation effect, caused by the high voltage which was close to the maximum operating voltage recommended by the manufacturer. By fitting a linear and polynomial function respectively the relative energy resolution could be calibrated.

The curves for the 3 and 1.5 inch PMT modules have been fitted by the linear function

$$\mu_{\text{lin}}(E_\gamma) = a_2 \cdot E_\gamma + a_1, \tag{4.1}$$

the 1 inch PMT was fitted using the polynomial function

$$\mu_{\text{pol}}(E_\gamma) = a_3 \cdot E_\gamma^2 + a_2 \cdot E_\gamma + a_1. \tag{4.2}$$

By using the derivative $\mu'(E_\gamma)$ of eq. 4.1 and 4.2 the sigma values can be calibrated by using the following relation

$$\sigma_{\text{cal}}(E_\gamma) = \frac{\sigma(E_\gamma)}{\mu'(E_\gamma)}. \tag{4.3}$$

The relative energy resolution can be calculated by:

$$\text{Energy Resolution}(E_\gamma) = \frac{\sigma_{\text{cal}}(E_\gamma)}{\mu(E_\gamma)} \cdot 100\%. \tag{4.4}$$

In Fig. 4.5 the calibrated relative energy resolution is shown for all three types of PMTs. The 3 and 1.5 inch PMT modules show a comparable relative energy resolution $4.76\%/\sqrt{GeV}$ and $5.76\%/\sqrt{GeV}$ respectively. The module which was equipped with a 1 inch PMT had the worst energy resolution ($7.78\%/\sqrt{GeV}$).

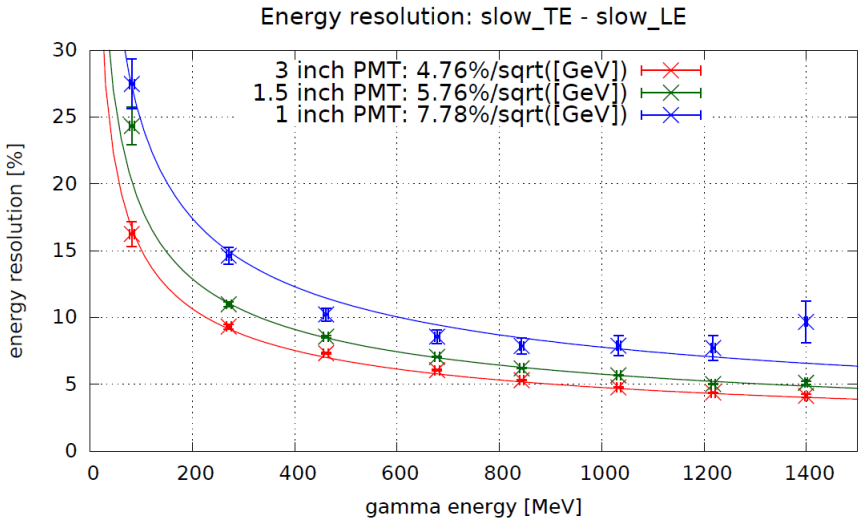


Figure 4.5: Calibrated relative energy resolution for all three PMT types.

The relative energy resolutions obtained by the PaDiWa-AMPS board have been compared with the Cracow ADC and the CAEN flash ADC reference measurements. The results for all three PMT types are shown in Fig. 4.6 - 4.8. All three electronics show comparable results. The relative energy resolution obtained with the Cracow ADC and PaDiWa-AMPS is slightly better than the CAEN + MA8000 setup what might be explained by a better optimization of the electronics to PMT pulse shapes.

4.2.2 Time Precision between Tagger and Scintillator

The time precision between the ECAL modules equipped with different PMTs and the Tagger trigger and the additional plastic sctinillator was studied. For that the time difference was calculated and fitted by a Gaussian function. The sigma value obtained by the fit is used to characterize the time precision. The results are shown in Fig. 4.9. The time precision between the plastic scintillator and the ECAL module is 750 ps. The time precision between the Tagger triggers and the ECAL module varies between 1300 ps and 450 ps. These results are not in agreement with measurements in the laboratory using cosmic muons. Here a time precision of about 250 ps between the trigger scintillaltor and the ECAL module has been obtained. The significantly worse time resolution during the beam time is explained by the signal processing electronics of the Tagger scintillators which was not optimized for fast timing.

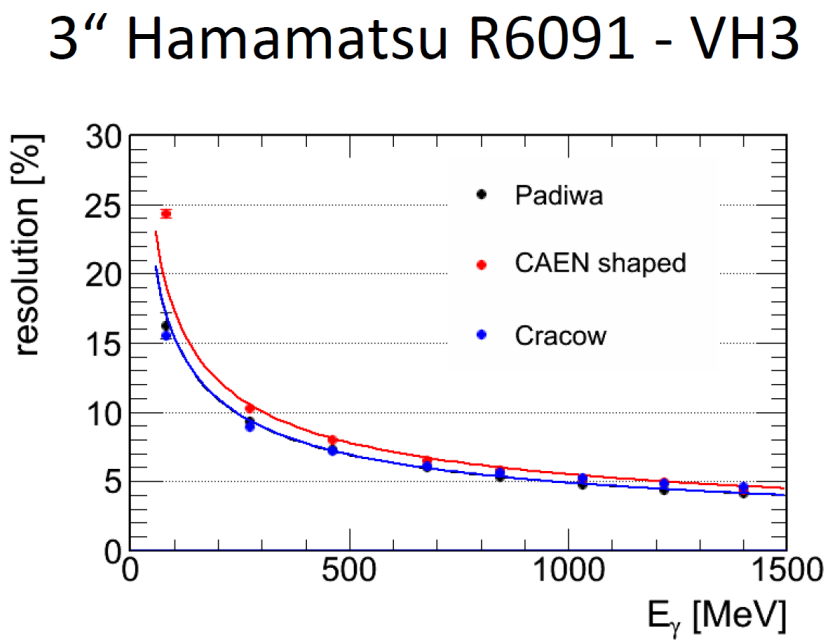


Figure 4.6: Comparison between all three tested read-out electronics for ECAL modules equipped with the 3 inch PMT types [50].

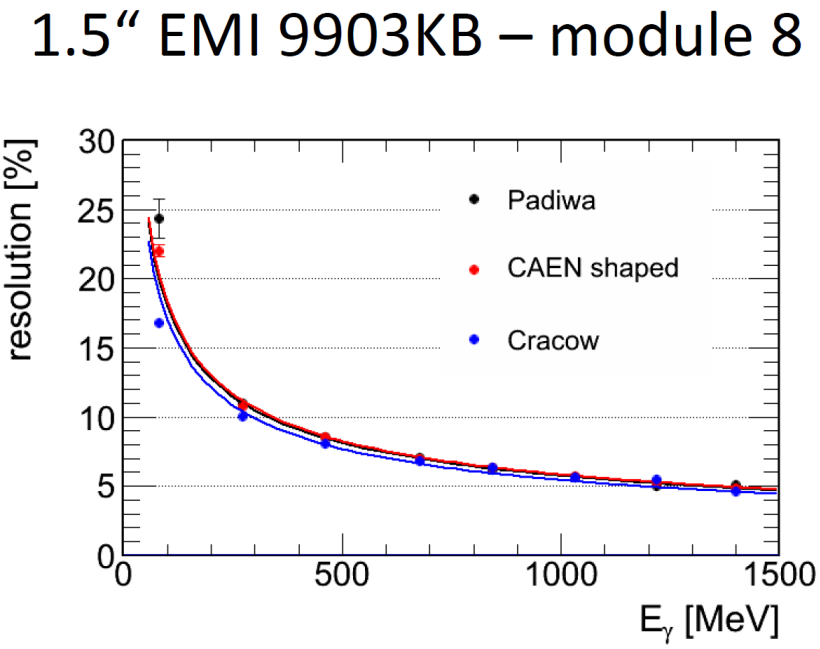


Figure 4.7: Comparison between all three tested read-out electronics for ECAL modules equipped with the 1.5 inch PMT types [50].

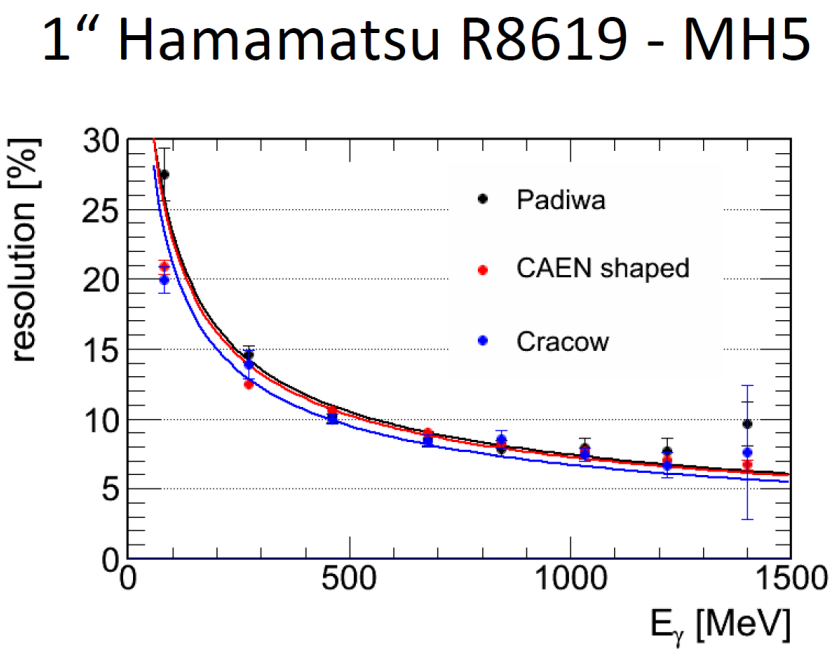


Figure 4.8: Comparison between all three tested read-out electronics for ECAL modules equipped with the 1 inch PMT types [50].

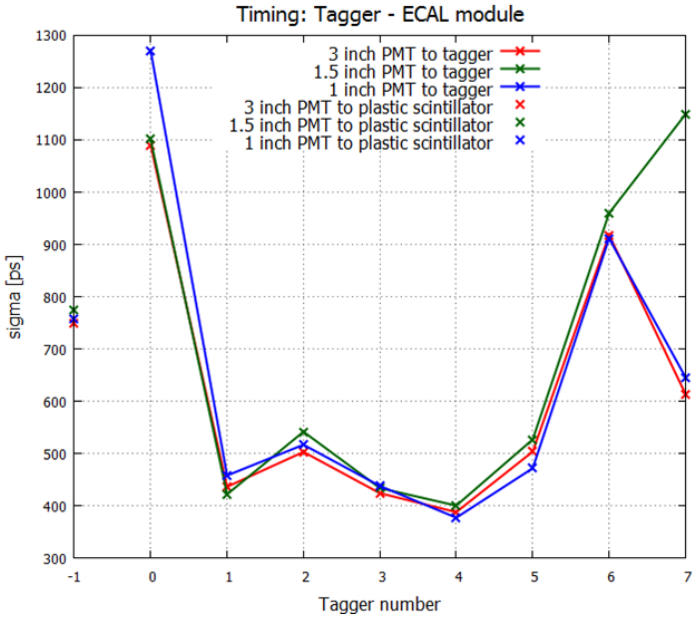


Figure 4.9: Time precision between the additional plastic scintillator and ECAL module (Tagger number -1) and between the eight Tagger channels and the ECAL module (Tagger number 0-7). The strong variation of the time precision indicates that the precision is dominated by the Tagger electronics.

5 Hodoscope PMT Read-out for the HADES Pion Beam Experiment

In July - August 2014 the HADES collaboration continued its physics program with pion beams. In addition a Hodoscope detector was installed in the HADES setup with the purpose of pion beam diagnostics. During the beam-time the flexibility of the PaDiWa-AMPS front-end was demonstrated. The PaDiWa-AMPS board was successfully adapted to the Hososcope PMT pulses which have a different pulse shape and a smaller amplitude range compared to those from ECAL PMTs. The adjustment process will be discussed in the following. With the measured timing data during the beam time a first estimation of the time precision between the Hodoscope and the HADES diamond based START detector was determined.

5.1 Adaption of the Attenuation Part to Hodoscope PMT Pulses

The pulse shapes from the 0.5 inch Hamamatsu R3478 PMTs, used in the Hodoscope, are different to those from ECAL PMTs. A typical Hodoscope pulse, obtained from a cosmic muon, is shown in Fig. 5.1. They are characterized by a relative fast rise-time which is of the order of 1 ns. The fall-time is about 10 ns which is four times smaller than HADES ECAL pulses. The amplitudes are about 250 mV, that is a factor of six smaller compared to ECAL pulses from cosmic muons. For this reason the attenuation of the PaDiWa-AMPS input had to be reduced.

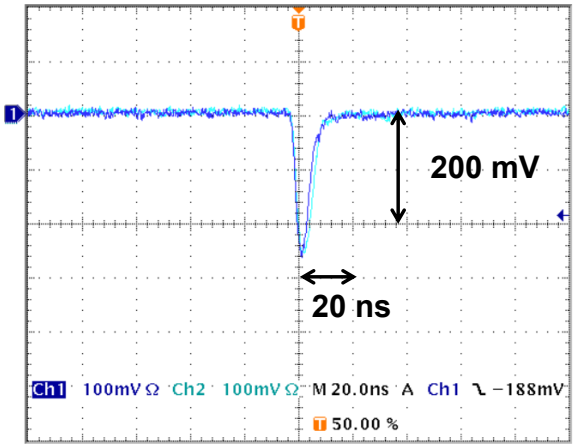


Figure 5.1: Hodoscope pulse shape generated by a cosmic muon. The plastic szintillators are read out from both sides using 0.5 inch Hamamatsu R3478 PMTs.

The location of the attenuation elements was shown the PaDiWa-AMPS schematics in Fig. 2.4. By modifying the values of two resistors it is possible to adapt the front-end to a different amplitude range. For adjustment to Hodscope pulses the value of R23 (see Fig. 2.4) was changed from 820 Ω to 180 Ω and the value of R25 (see Fig. 2.4) from 53.6 Ω to 68 Ω. This change increased the amplification by a factor of 4.2. Furthermore the values have been chosen to keep the input impedance at 50 Ω. Because of the small pulse width the starting point of the DISCHARGE signal had also to be adjusted. At this time the delay could be slightly modified by routing the DISCHARGE signal out of the FPGA, through an array of capacitance, and back into the FPGA. By optimizing the VHDL code the delay of the DISCHARGE signal could be decreased. The delay between the rising edge of the FAST signal and the rising edge of the

DISCHARGE signal is about 25 ns in the Hodsocope FPGA design. In comparison, the ECAL FPGA design implements a delay of about 40 ns. In section 6.3.2 a more flexible and adjustable delay, which is based on the delay time of the DISCHARGE signal inside the FPGA, will be introduced. During the beam-time only basic modifications of the FAST channels have been done to adapt it to Hodoscope PMTs. The integrator part (SLOW channels) has not been optimized at this time. In section 6.2 several suggestions for an optimization of the integrator part, based on SPICE simulations, will be given.

5.2 HADES Hodoscope Read-out during the Pion Beam Experiment

The Hodoscope was located in the HADES pion beam experiment 6 m downstream of the Start detector (see Fig. 1.3). A photography of the Hodoscope setup is shown in Fig. 5.2. A movable support frame was build out of aluminum profiles which houses the Hodoscope, HV-Supply and the read-out electronics. Four PaDiWa-AMPS front-end boards and one TRB3 have been used to read out the 32 PMTs of the Hodoscope. To gain the maximum in time precision and therefore the optimal x-position resolution of the Hodoscope, left and right side PMTs have been connected to the same PaDiWa-AMPS board.

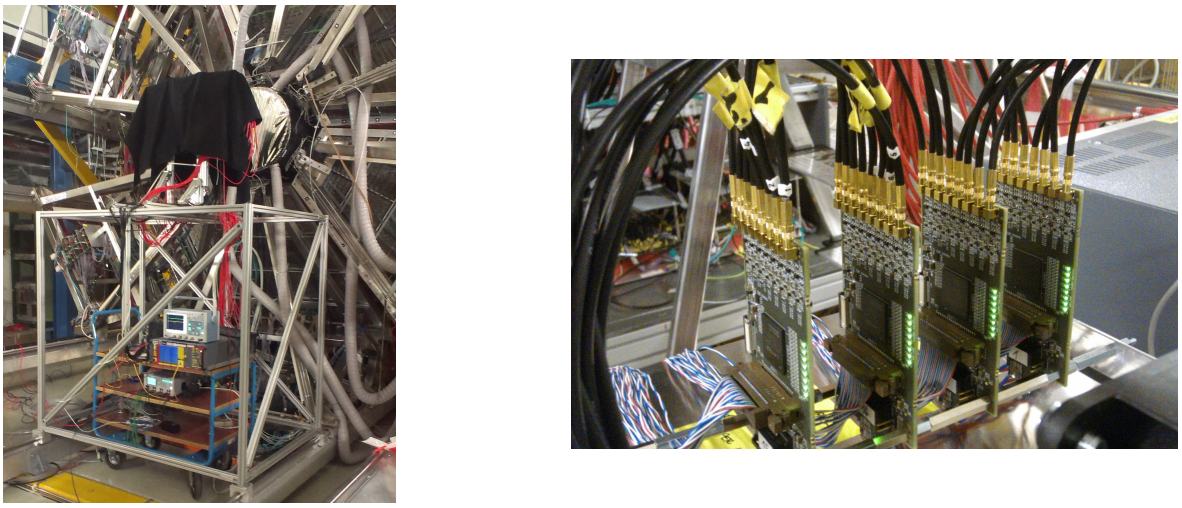


Figure 5.2: Left panel: Hodscope detector set-up seen from the back side of the HADES. The movable platform contains the Hodoscope (covered with a black blanket), HV-Supply and read-out electronics. **Right panel:** Four modified PaDiWa-AMPS boards in combination with a TRB3 have been used to read out the 32 channels of the Hodoscope detector.

5.2.1 Pion Beam Monitoring

The Hodsocope was used during the pion beam in combination with the CERBEROS [13] pion tracking system for pion beam monitoring. The Hodoscope was used to monitor the pion beam position at the end of the HADES detector. Due to its segmentation into 8 rods and the PMT readout on both sides a position information in x- and y-direction could be obtained. The quality assessment (QA) plots were displayed in real time in the HADES control room and gave an information of the location of the beam. This was especially needed for the alignment of the pion beam. Two QA plots are shown in Fig. 5.3. The hit rate from each PMT is shown in Fig. 5.3 (left panel). The hit rate of all eight rods as function of the time, which is shown in Fig. 5.3 (right panel), shows the spill structure of the beam.

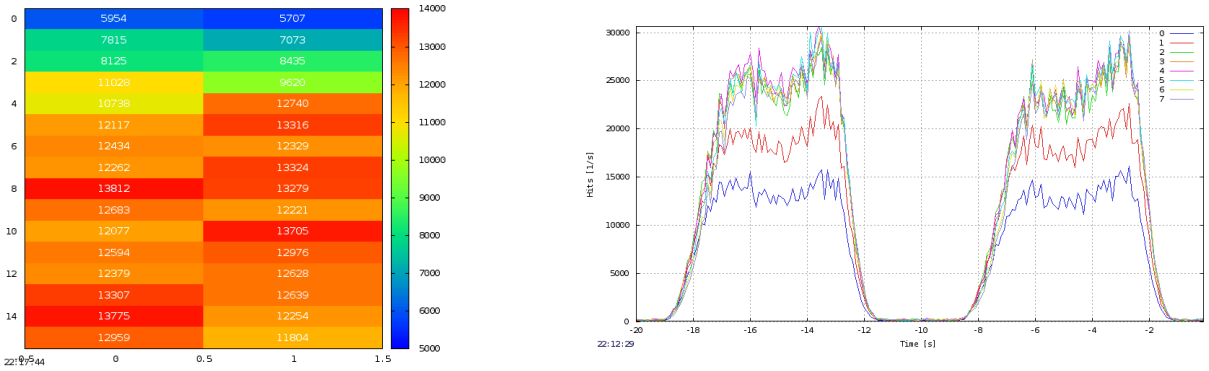


Figure 5.3: Examples of two quality assessment (QA) plots which have been displayed in the HADES control room during the pion beam time. **Left panel:** The hit rate per second is displayed for all PMTs of the Hodoscope. The y-profile of the beam is visible. **Right panel:** Hit rate of all eight rods as a function of time. The spill structure of the pion beam is visible.

5.2.2 Determination of the Time Precision between Hodoscope and Start Detector

The Hodoscope was also used to determine the time precision between the Hodoscope and the START detector. A detailed discussion can be found in [6]. The time precision between Hodoscope and Start detector was determined by using pions hitting the Start detector at the time t_O and the Hososcope at time t_1. The time of flight can be calculated by the simple formula

$$\Delta t = t_1 - t_0. \tag{5.1}$$

The measured time of flight is about 19 ns. The distribution was fitted by a Gaussian function and its σ value was used for the characterization of the time precision between both detectors. Assuming that $\sigma_{\text{Hodoscope}} = \sigma_{\text{Start}} = \frac{\sigma}{\sqrt{2}}$ a time precision of 250 ps was obtained for the Hodoscope and the Start detector respectively. A better time resolution is obtained by selecting only pions which hit the central parts of the Hodoscope. For that the time difference between both rods was calculated which allows to get information of the x-position. The position measurement is shown in Fig. 5.4 in which the central events are marked by Cut1.

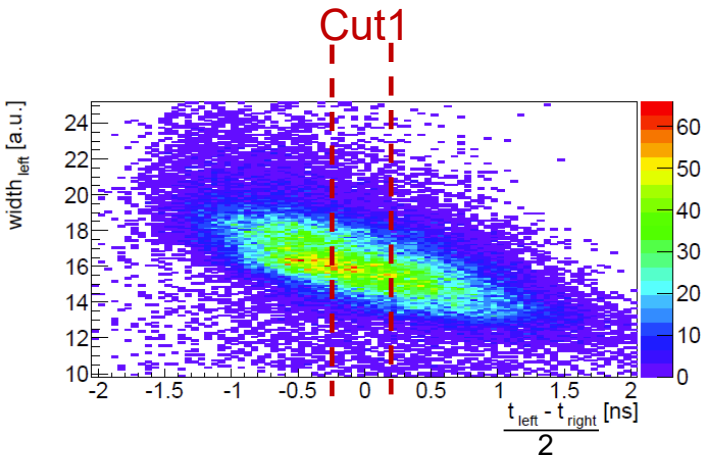


Figure 5.4: Walk effect of the position measurement along a Hodoscope rod. The time difference between left and right read out PMT as a function of the SLOW signal width (Q2ToT) is shown. **Right panel:** Time of flight measurement between Hodoscope and Start detector without corrections. For more details see [6].

The time-of-flight distribution for the central events (Cut1) is shown in Fig. 5.5. With the selection of pions, detected in the central region of the detector, the time resolution could be slightly improved to 234 ps. By applying additional corrections (i.e. corrections of time walk effect of the Start Detector) the time precision of both detectors could be estimated to be 173 ps [6]. One has to mention that both detectors have been assumed to have the same contribution to the total time precision. The real contribution of each detector is not quantifiable separately with this approach.

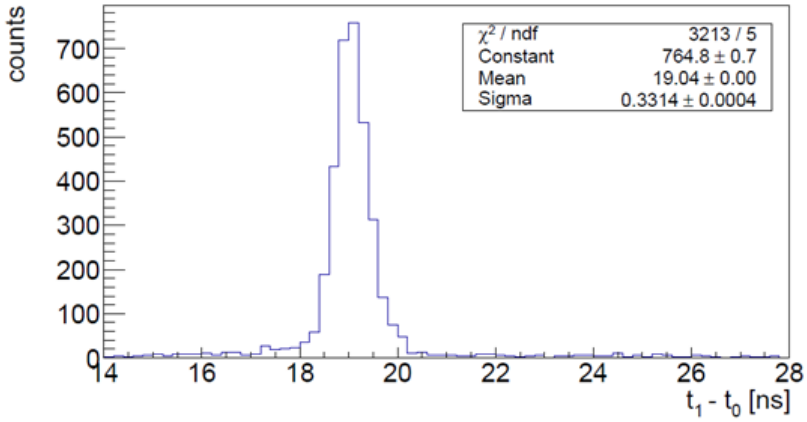


Figure 5.5: Time of flight measurement between Hodoscope (t_1) and Start detector (t_2) including the Cut1 correction. For more details see [6].

6 Optimization of PaDiWa-AMPS for PMT, Si-PM and Diamond Detector Read-out

In this chapter the optimization process of the PaDiWa-AMPS front-end board is discussed. The analog electronic scheme was optimized to gain a maximum in terms of time and charge precision, dynamic range, signal-to-noise ratio and rate capability. For that SPICE simulations (see appendix 8.3) in combination with measurements in the laboratory have been performed. Besides ECAL PMT read-out two other potential read-out applications for the HADES and the CBM experiment will be introduced. At present the electronic is adapted for Silicon Photomutpliers (Si-PM) signals which are foreseen to be used as read-out of the Projectile Spectator Detector (PSD) of the CBM experiment. There are also plans to use this concept to read out Diamond Detectors which will be used in the HADES and the CBM experiments. The analog electronic optimizations of the PaDiWa-AMPS board, which were mentioned above, are presented for all three detector types. Moreover, besides optimization of the analog part of electronics, the VHDL code of the PaDiWa-AMPS FPGA was modified. In the generation of the DISCHARGE signal improvements have been made. An additional flexibility via adjustable delays of the DISCHARGE signals was implemented.

6.1 Motivation for Si-PM and Diamond Detector Read-out

The experience gained in the laboratory tests and in beam measurements showed that due to the flexibility of the analog part of the PaDiWa-AMPS front-end board several applications besides ECAL PMT read-out are possible. In the following section the read-out of Si-PMs and Diamond Detectors are motivated. Typical signals, which are important for the adjustment process of the PaDiWa-AMPS board, are shown for both detector types.

6.1.1 Si-PM Read-out - The Projectile Spectator Detector (PSD) for the CBM Experiment

The Compressed Baryonic Matter (CBM) Experiment [54] which is planned for the future FAIR accelerator complex will explore the nuclear phase diagram in the region of high net-baryon densities. A Projectile Spectator Detector (PSD) [55] is needed to determine the collision centrality and the orientation of the reaction plane. For this purpose a "shashlik" type lead-scintillator hadron calorimeter is foreseen. Charged particles generate a particle shower inside the lead material. The shower particles are then detected with help of the scintillation material. The generated photons in the scintillator material are collected and transported via wavelength shifting fibers to silicon photomultipliers (Si-PMs).

A silicon photomultiplier (Si-PM) is a generic name for silicon based single photon sensitive devices built from an avalanche photodiode (APD). The Hamamatsu S12572 multi-pixel photon counter (MPPC), which is one representative of these devices, is considered as potential candidate to read-out the PSD detector. The signals from the Si-PMs have to be pre-amplified before they are read out by a front-end electronics. The pre-amplifier has also the task to provide the required bias voltage which is in the order of typically 25 V - 95 V. A signal from a Hamamatsu S12572 MPPC is shown in Fig. 6.1. The pulse was generated by illuminating the Si-PM with a short LED light pulses. The signal is characterized by a relative slow full rise-time which is about 6 ns - 8 ns. The full fall-time is about 50 ns. This results in a full width of about 60 ns. The amplitude range which needs to be covered by the read-out electronics is between 4 mV and 2000 mV. Si-PMs and specially the pre-amplifiers are very sensitive to external noise which puts an additional requirement on robustness of the read-out electronics.

The NA61/SHINE Experiment [56] which is located at the CERN SPS in Geneva is equipped with a PSD similar to the one planned to be built for the CBM experiment. A synergy between the CBM and the NA61/SHINE collaboration opens the possibility for common research and development of the PSD detector and the read-out electronics. A benefit of this tight collaboration is that beam tests can be performed on a running experiment.

Tests with a PSD prototype module, which is located in the GSI Detector Laboratory, and the PaDiWa-AMPS front-end are currently ongoing. First steps of the optimization process are discussed in section 6.2. A beam test at the NA61/SHINE PSD, with an optimized PaDiWa-AMPS version for Si-PM read-out, is planned for mid of 2016.

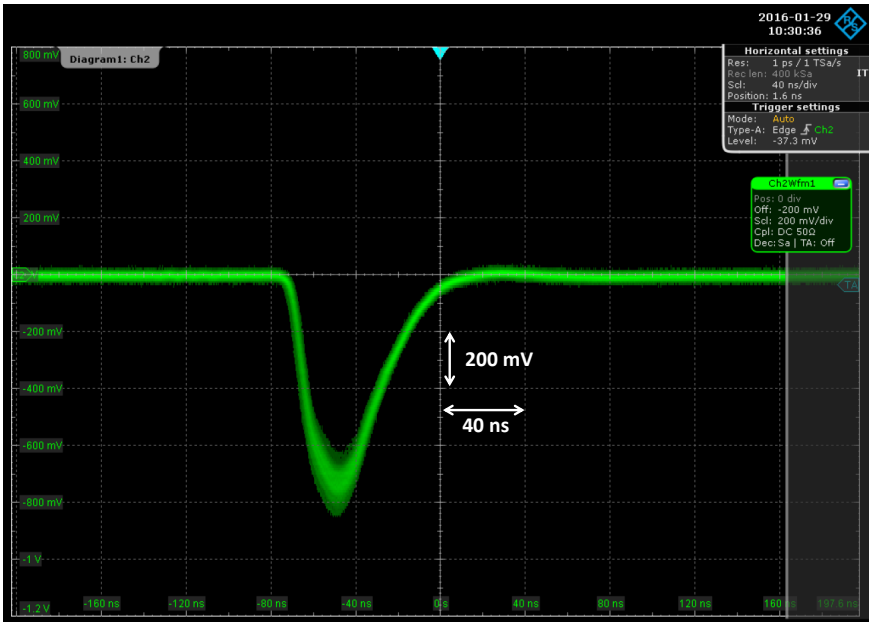


Figure 6.1: Si-PM pulse generated by a Hamamatsu S12572 MPPC which was irradiated with short LED pulses.

6.1.2 Diamond Detector Read-out for the HADES and CBM Experiments

The concept of a Diamond Detector was already introduced in section 1.2. For the HADES and the CBM experiments the Start-Veto System is/will be based on single-crystal Chemical Vapour Deposition (scCVD) diamond material. A large area of several hundred mm^2 has to be covered with a fine segmentation of the diamond detector in order to extract an information on position for beam monitoring purpose. Beside this diamond detectors are used for precise time measurements of the start time of the reaction. Challenging are the high rate requirements up to $10^8\,(s \cdot mm^2)^{-1}$ which have to be met by the material, as well as by the read-out electronics (about $10^7\,s^{-1}$ per channel).

Because diamonds are also used for time-of-flight measurements and triggering a precise time measurement is absolutely important. Besides time, a charge information is also useful. In Fig. 6.2 the radiation damage of a diamond detector which was used during the HADES Au+Au run is shown. The diamond was irradiated during 150 hours with an 1.25 AGeV Au beam which is equivalent to a total dose of 87 MGy [8]. The diamond was scanned with an proton micro-beam and the detector response measured. A clear reduction of the amplitude could be observed in the damaged areas. This motivates the need of a charge measurement in order to monitor the damage during the beam time. Furthermore a precise charge measurement gives also the opportunity to veto heavy beam fragments which pass without an interaction in the target.

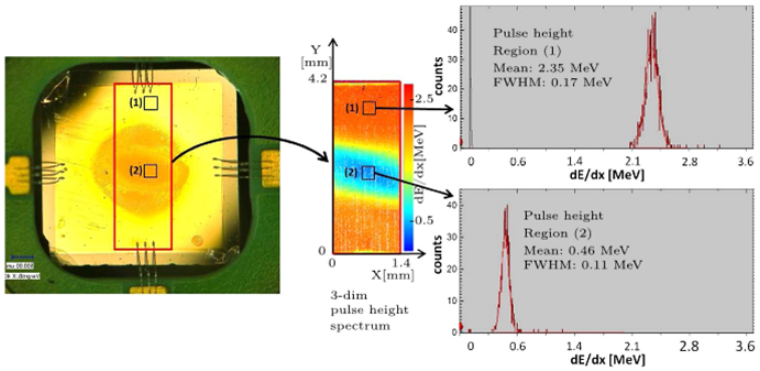


Figure 6.2: Left panel: HADES Diamond detector after irradiation with Gold ions. **Middle panel:** The distribution of energy loss of pulse height spectrum. **Right panel:** Pulse height for two regions on the diamond. Top panel: less irradiated area, bottom panel highly irradiated area [8].

In Fig. 6.3 a typical signal generated by a Diamond Detector is shown. A monocrystalline diamond material with a thickness of 500 μm was irradiated with a Strontium-90 source. A preamplifier in combination with a second booster/shaping amplifier was used. The signal is characterized by a relative fast full rise-time which is in the order of 1 ns. The full fall-time is in the order of 6 ns which results in a base width of about 10 ns.

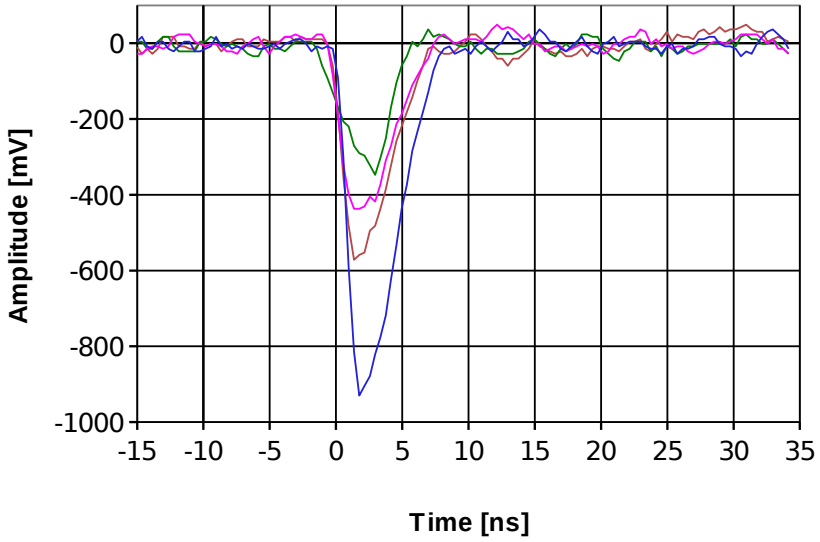


Figure 6.3: Pulse shapes from 500 μm thick mono crystalline diamond detector which is irradiated with a Sr-90 source (equivalent to MIPS), measured after pre-amplifier & booster/shaper amplifier.

6.2 Optimization for PMT, Si-PM and Diamond Detector Applications via Spice Simulations

The analog stage of the PaDiWa-AMPS board can be adjusted to pulses generated by ECAL PMTs (see Fig. 1.15), Hodoscope PMTs (see Fig. 5.1), Si-PMs (see Fig. 6.1) and Diamond Detectors (see Fig 6.3). For that SPICE simulations (see appendix 8.3) in combination with laboratory tests have been done for all detector types. The signal-to-noise ratio and the integrator were optimized. The low and high frequency cut-offs were adapted to all pulse shapes. Beside this the baseline return of the integrator could be optimized. The modifications and the simulation results are shown in the following.

In order to optimize the signal-to-noise ratio, the frequency dependence of the amplification stages need to be adapted to fit to the rise-time of the different detector signals. A cutting off external and

internal noise in frequency ranges, which are not relevant for the signal amplification, has to be done. It should be mentioned that the frequency range should not be too narrow to avoid signal distortions. For example a narrow spike-like distribution in the frequency space results in a sinusoidal oscillation in the time space. Since the noise at a constant gain typically increases with $\sqrt{f}$, the contribution of high frequencies are dominant in the integrated noise. In order to obtain the best time resolution ΔT for the FAST signal, the ratio

$$\Delta T = \frac{(\text{pulse risetime}) \cdot (\text{noise amplitude})}{(\text{pulse amplitude})} \tag{6.1}$$

has to be optimized. This expression does not contain the intrinsic behavior of a variation of the signal arrival and rise-time due to the intrinsic properties of the detector.

6.2.1 Optimization of high Frequency Cut-off - Low Pass Filter

In the following the Low Pass Filter (see Fig. 2.4) is optimized via SPICE simulations in parallel for signals of all three considered detector types.

ECAL PMT Signals

In Fig. 6.4 the simulated frequency as a function of the electronic normalized noise (noise amplitude)/$\sqrt{f}$ is shown for two different values (2.7 pF and 6.8 pF) of the filtering capacitor C258 (see Fig. 2.4). The filtering capacitor is located directly behind the transistor of the first amplification stage. The sharp high frequency cut-off which is observed for the larger capacitor value reduces the integrated noise by 20%. It should be mentioned that the feedback resistor R21 between collector and base of the transistor of the first amplification stage (see Fig. 2.4) was increased from 680 Ω to 1 kΩ in this simulation. This results also in a reduction of the gain for very high frequencies where the gain in the region of interest (100 kHz - 200 MHz) increases

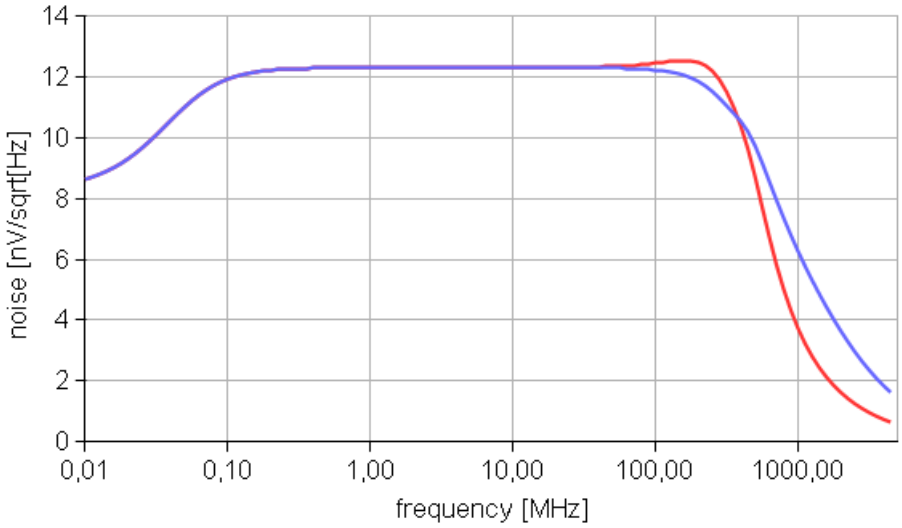


Figure 6.4: Frequency dependence of the normalized noise at the output of the FAST amplification stage for two values of the filter capacitor C258. Blue curve: 2.7 pF, Red curve 6.8 pF.

The corresponding simulated amplified FAST signals for both filtering capacitors are shown in Fig. 6.5. A total rise-time of 2 ns is used for the input signal. This is a bit faster than the measured rise time of an ECAL PMT pulse. The frequency dependence of the normalized electronic noise in Fig. 6.5 shows no

difference in the rise-time. Thus the signal-to-noise ratio which affects the intrinsic time resolution is improved also by 20%. The slightly increased gain at frequencies around 100 MHz (typical frequency range relevant for the signal rise-time) results in a slightly larger signal amplitude. Thus, the original filter capacitance of 2.7 pF was increased to 6.8 pF. Depending on the frequencies content in the external noise, this value could be increased even further.

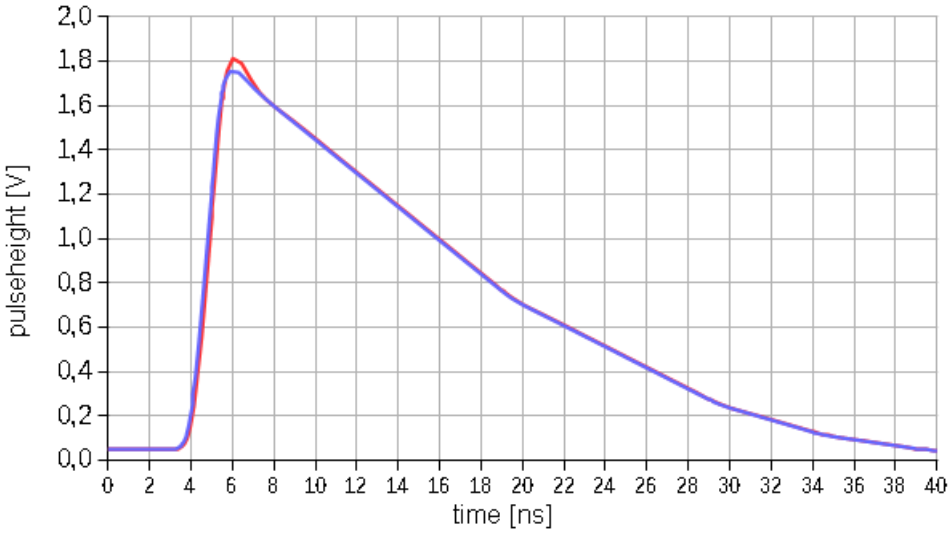


Figure 6.5: Amplified FAST signal for two values of the filtering capacitor C258. Blue curve: 2.7 pF, Red curve: 6.8 pF. The total rise-time of the input signal is 2 ns which is comparable to ECAL PMTs.

PSD Si-PM Signals

For signals from Si-PMs the high frequency cut-off of the FAST amplifier was optimized in the same way as for the ECAL PMTs. The rise-time of the signals as compared to those from ECAL PMTs are by a factor 2 larger. Furthermore, the Si-PM and their pre-amplifier produces additional noise in the high frequency range which needs to be suppressed. This result in a significantly larger filter capacitor C258 at the output of the first amplification stage (see Fig. 2.4). Again in this simulation the feedback resistor R21 of the first amplification stage was increased from 680 Ω to 1 kΩ. A reduction of noise at higher frequencies as well as a higher gain results from the latter optimization. In Fig. 6.6 a comparison of the frequency dependence of the normalized electronic noise is shown for two different values (2.7 pF and 47 pF) of the filter capacitor C258. The filtering capacitor with a value of 47 pF reduces the integrated noise compared to the original value down to 50%.

The corresponding simulated amplified FAST signals are shown for both filtering capacitors in Fig. 6.7. A total rise-time of 5 ns is used for the input signal. This is in the order of the rise-time of a Si-PM pulse. The larger filtering capacitor generates a delay of the input signal which is in the order of 1 ns. Also the rise-time is slightly increased by less than 0.2 ns. This results in an improved intrinsic time resolution of about 40%. However, the time-resolution of the detector which is typically in the order of several 100 ps dominates the total time resolution.

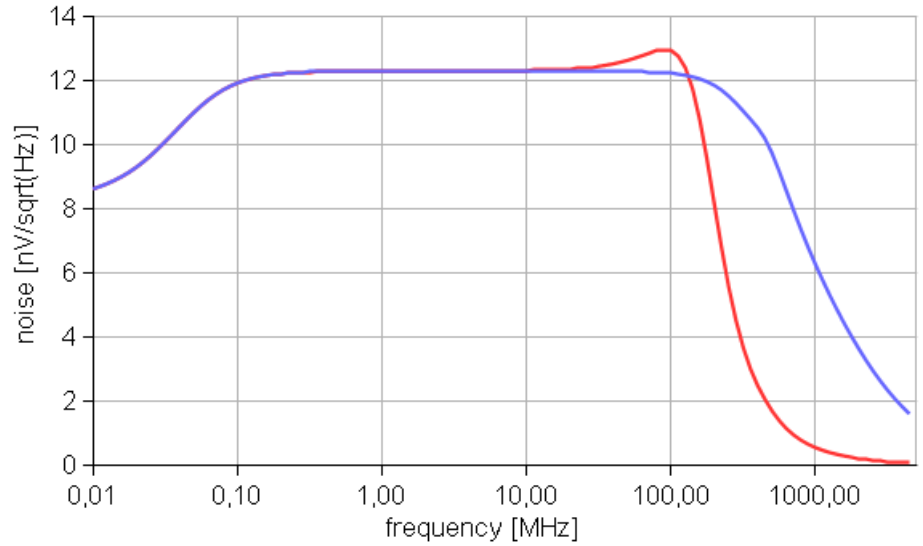


Figure 6.6: Frequency dependence of the normalized noise at the output of the FAST amplification stage for two values of the filter capacitor C258. Blue curve: 2.7 pF, Red curve: 47 pF.

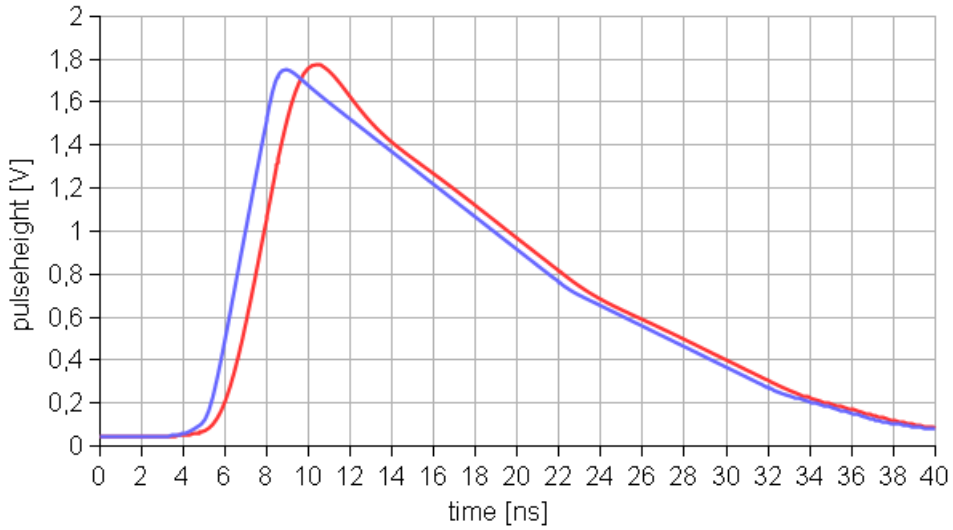


Figure 6.7: Amplified FAST signal for two values of the filtering capacitor C258. Blue curve: 2.7 pF, Red curve: 47 pF. The total rise-time of the input signal is 5 ns which is comparable to PSD Si-PM signals.

Diamond Detector and Hodoscope PMTs

The small 0.5 inch PMTs used in the Hodoscope provide much faster and shorter signals as compared to those from ECAL PMTs. They have a similar pulse shape, even a bit wider, compared to the signals of diamond detectors which are generated by minimum ionizing (MIPS) particles. Thus, the following simulation holds for both detector types. In Fig. 6.8 the frequency dependence of the normalized electronic noise output of the first amplification stage (see Fig. 2.4) is shown for different filter capacitors of 1 pF and 2.7 pF, respectively. The feedback resistor R21 of the first amplification stage remained unchanged. The lager filtering capacitor reduces the integrated noise compared to the original value by 21%.

The corresponding simulated amplified FAST signals are shown for both filtering capacitors in Fig. 6.9. The smaller capacitor of 1 pF does not improve the rise-time. The slight increase of the gain at frequencies

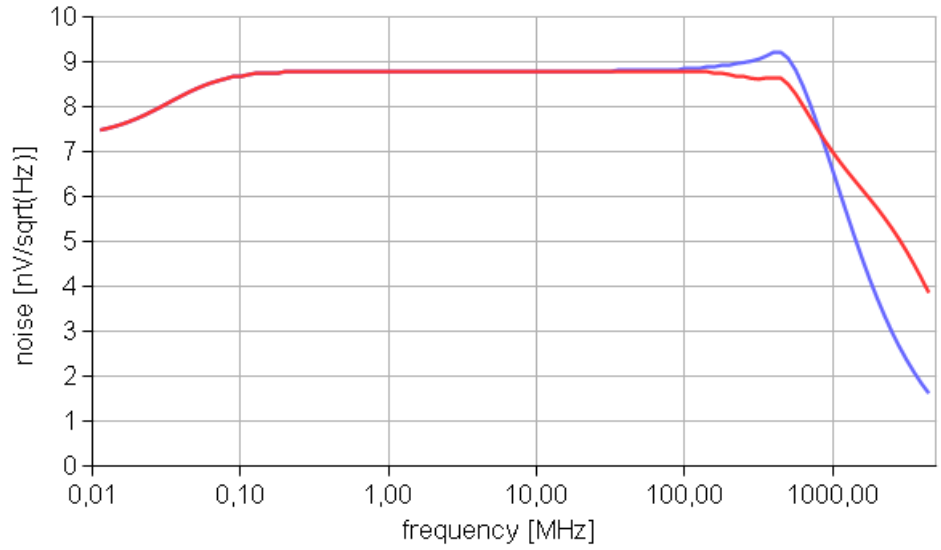


Figure 6.8: Frequency dependence of the normalized noise at the output of the FAST amplification stage for two values of the filter capacitor C258. Blue curve: 2.7 pF, Red curve: 1 pF.

of 500 MHz for the 2.7 pF capacitance (see Fig. 6.8) results in slightly larger amplitude of the FAST output signal. The 2.7 pF capacitor which is used in the original PaDiWa-AMPS prototype is obviously well suited for this type of signals.

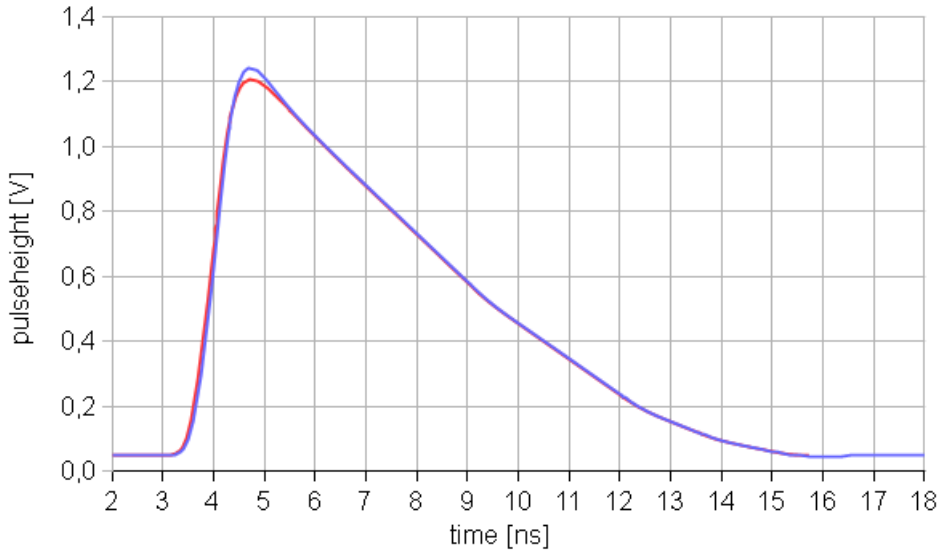


Figure 6.9: Amplified FAST signal for two values of the filtering capacitor C258. Blue curve: 2.7 pF, Red curve: 1 pF. The total rise-time of the input signal is 1 ns what is comparable to a Diamond or a fast Hodoscope PMT signal.

6.2.2 Integrator Optimization - Matching of FAST and SLOW (integrator) Gain

To provide an optimal dynamic range for input pulses, the maximum pulse-height accepted by the FAST amplifier and the SLOW integration stage should be matched. The FAST amplifier starts to saturate at a pulse-height of the FAST output of about 4 V. The integrator is sensitive to the total charge i.e. the product of signal height and signal widths. Thus, for width of the detector signal which differ significantly from

those from ECAL PMTs the integrator sensitivity needs to be adjusted. This is the case for the short Hodoscope PMT and diamond detector signals as well as for the wider Si-PM signals of the PSD. In the following simulation results for a better matching of FAST and SLOW will be shown.

PSD Si-PMs

The amplitude of the integrator SLOW output for a given input pulse-height can be reduced by choosing a larger integrating capacitor C262 (see Fig. 2.4) and/or by a smaller termination resistor R122 (see Fig. 2.4). The result of a simulation is shown in Fig. 6.10. An input signal with an amplitude of 2 V, which is about factor of 2 below the saturation point of the FAST amplifier, was used. Due to the large pulse width, the integrated SLOW output is already saturated (see blue curve in Fig. 6.10). Even at saturation, the pulse width of the integrator output increases with increasing amplitude of the input signal. A Q2ToT measurement is still possible but the response is getting non-linear (see section 3.4). By increasing the integrating capacitor from 10 nF to 12 nF and decreasing the termination resistor from 220 Ω to 200 Ω, the saturation of the 2 V input pulse is avoided. Due to the corresponding reduction of noise, the resolution of the integrator is not affected. The reduced area of the integrator SLOW output signal results also in a reduced overshoot after the DISCHARGE signal is turned off.

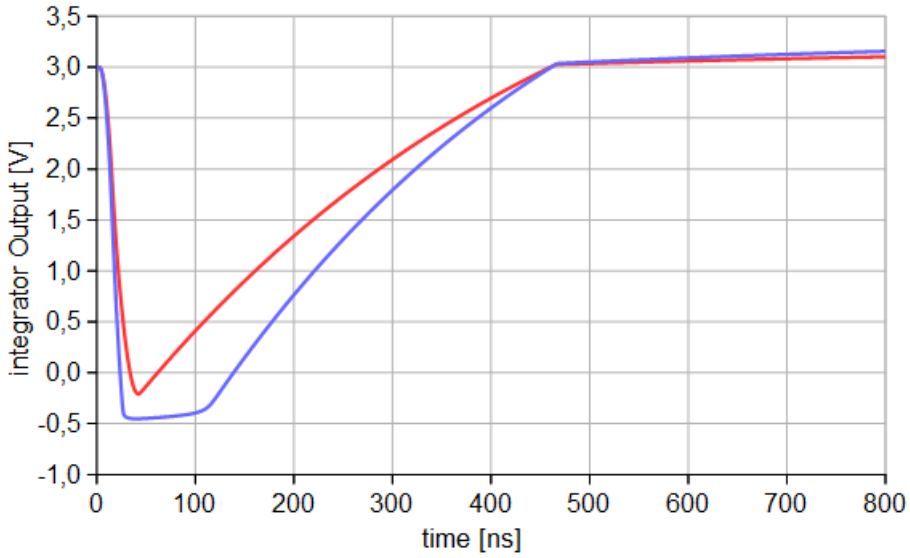


Figure 6.10: Simulated SLOW output for a typical PSD Si-PM signal with an amplitude of 2 V. The result for the standard ECAL version is shown with the blue curve. The integrating capacitor is increased from 10 nF to 12 nF and the termination resistor is reduced from 220 Ω to 200 Ω. The resulting signal shown with the red curve does not indicate saturation.

Diamond Detector and Hodoscope PMTs

As compared to ECAL PMT signals, the width of Hodoscope PMTs and diamond detector signals is much smaller. Thus, the integrator SLOW output amplitude for a given input signal amplitude is significantly reduced. To obtain a better matching of the pulse height between FAST and SLOW output signals, the value of the integration capacitor C262 (see Fig. 2.4) needs to be reduced and the termination resistor R122 (see Fig. 2.4) needs to be increased. In Fig. 6.11 a simulation result is shown. The resulting SLOW output signal of the integrator is increased by nearly factor of 2 compared to the original ECAL PMT version of the board.

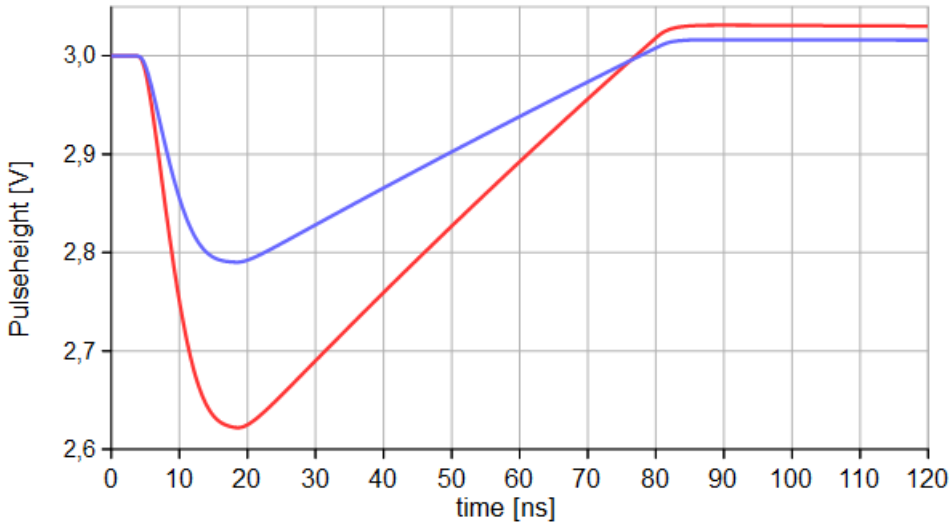


Figure 6.11: Simulated SLOW output for a typical Hodoscope or Diamond Detector signal with an amplitude of 0.5 V. The result for the standard ECAL version is shown with the blue. The integrating capacitor is decreased from 10 nF to 6.8 nF and the termination resistor is increased from 220 Ω to 270 Ω. The resulting signal with the red curve shows the higher gain of the integrator.

6.2.3 Optimization of the low Frequency Cut-off - High Pass Filter

It turned out that external low frequency noise limits the precision of the charge measurement and negatively influences the threshold setting of the SLOW integrator channel and therefore the dynamic range. The integrator is sensitive to low frequency noise per se. Even small amplitudes integrated over a long time period can result in sizable shifts of the baseline. Thus, a low frequency cut-off already at the first FAST amplification stage needs to be optimized. Thereby the DISCHARGE signal should stay constant without a distortion during the complete discharge of the integrator capacitance (typically of the order of few 100 ns).

Simulations in combination with pulser based laboratory investigations have been done to optimize the low frequency cut-off. Best results were achieved by reducing the inductor L4 at the collector of the FAST amplification transistor (see Fig. 2.4), which serves as a high pass filter. The inductance was reduced from L4 = 330 μH down to 100 μH and even lower to 47 μH. While the latter setting distorted the DISCHARGE signal in an unreasonable way, the 100 μH turned out to be a suitable choice. In Fig. 6.12 the integrator gain as a function of frequency for an inductor value of the originally implemented L4 = 330 μH and the optimized value of 100 μH is shown. A gain reduction of about 50% is visible in the low frequency range of a few 10 kHz. In laboratory test it was found that low frequency noise which is introduced by the laboratory pulsers could be significantly reduced. At the same time, the pulse shape of the integrated SLOW signal is not affected from the change of the inductance (see Fig. 6.13).

From this behavior one can conclude that the dynamic range of the integrator as described in section 3.4 can be significantly improved. However, the influence of external low frequency noise depends on proper grounding and shielding which are needed to minimize external noise pickup.

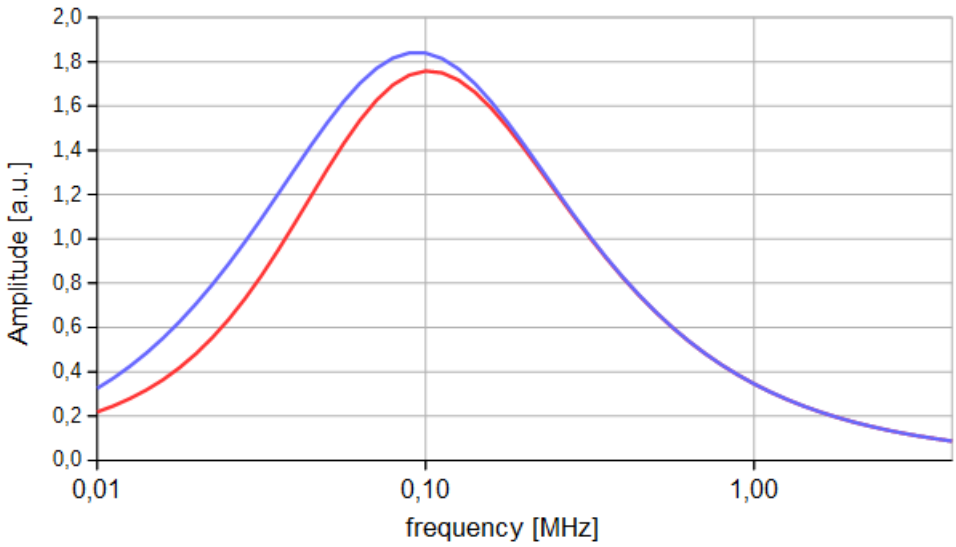


Figure 6.12: Frequency dependence of the gain of the SLOW integrator for two different values of the blocking inductor L4. Blue curve: $L4 = 330\,\mu H$, Red curve: $L4 = 100\,\mu H$. A gain reduction of about 50% in the low frequency range of a few 10 kHz is visible.

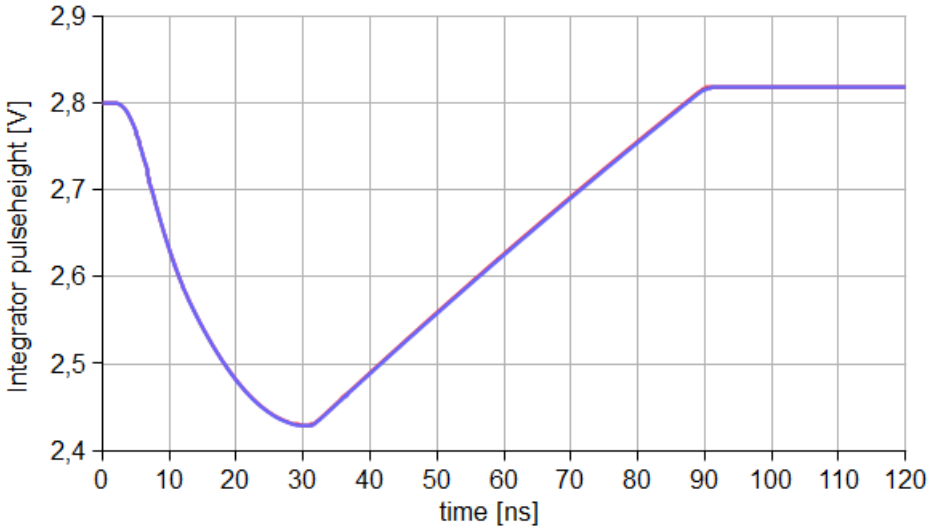


Figure 6.13: Integrated SLOW output signal simulated for an ECAL PMT shaped input signal with an amplitude of 0.7 V for two different values of the blocking inductor L4. Blue curve: $330\,\mu H$, Red curve: $100\,\mu H$. Blue curve and red curve fall on top of each other.

6.2.4 Optimizing the Baseline-return of the Integrator

As already mentioned in section 3.5 the overshoot which is present in the integrated SLOW signal, limits the rate capability of the front-end electronics. This overshoot has a quite large decay time which is in the order of several μs. Thus, the rate capability is limited to about 100 kHz. Simulations in combination with laboratory tests have been done to reduce the decay time. In Fig. 6.14 a simulation for two different blocking inductance L6 and L7 (see Fig. 2.4) are shown. By replacing the 660 μH blocking inductance by 330 μH the overshoot decay time could be reduced. It has to be mentioned that only an active baseline restorer can reduce the decay time significantly. An active baseline restorer implemented inside the FPGA could be a possible solution. The idea is as follows: the DISCHARGE signal should be

extended as a function of its original width based on a FAST counter which is implemented in the FPGA. Afterward the signal is inverted to force the integrator baseline back to its normal value. This results in a much faster baseline recovery avoiding long exponential tails of the unavoidable overshoot. Besides the implementation in the VHDL code, the layout of the PadiWa-AMPS board has to be redesigned. The location of the in- and out-put pins of the FPGA has to be optimized regarding the timing performance. The redesign with all above mentioned optimizations is been currently produced and will become available by mid of 2016.

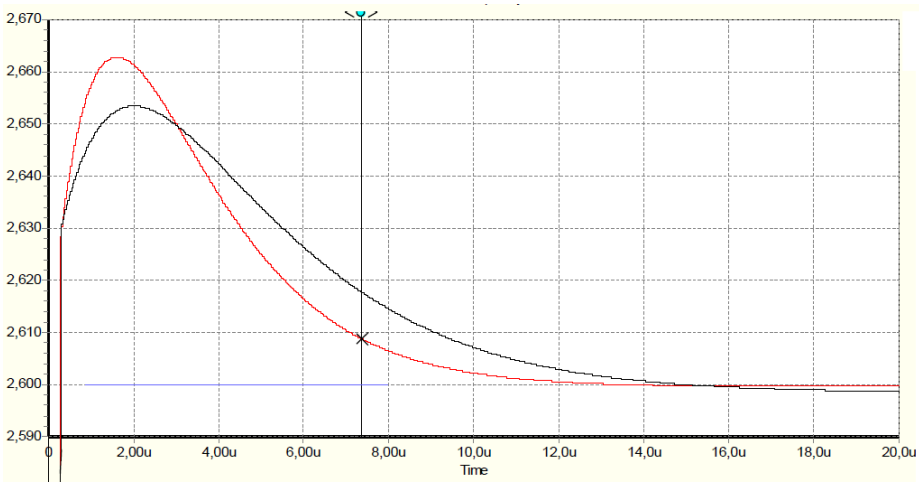


Figure 6.14: The decay time of the overshoot can be reduced by replacing the 660 μH (black) blocking inductance (L6 + L7, see 2.4) by 300 μH (red). This allows a higher rate capability.

6.3 VHDL Code Optimizations

The generation of the DISCHARGE signal which is used to discharge the integration capacitor was optimized. For that two major improvements have been made in the VHDL code of the PaDiWa-AMPS FPGA. On the one hand the release condition of the DISCHARGE was improved to make it more robust against re-triggering on the integrator output at low threshold settings. On the other hand a selectable delay of the DISCHARGE signal was implemented. This allows a flexible adjustment to the pulse width of the input signals.

6.3.1 Release Condition of the DISCHARGE Signal

The DISCHARGE signal is used to discharge the integration capacitor with the help of a constant current source using a standard FPGA output. In the first version of the VHDL code the DISCHARGE signal was triggered by a logical OR between the delayed leading edge of the FAST signal and the leading edge of the SLOW signal. This is not the ideal way, because the DISCHARGE signal could be triggered by a leading edge in the SLOW channel without having a leading edge in the FAST channel. This case can happen for example due to noise in the SLOW channel. Furthermore a problem occurred, when the threshold of the SLOW channel is set to a very low relative threshold, an oscillation was observed in the SLOW signal due to continuous re-triggering. In Fig. 6.15 (left panel) the observed oscillation in the SLOW signal is shown. The oscillation can be explained by re-triggering on the SLOW signal due to a signal undershoot following the integrated signal after discharging. This undershoot is related to the overshoot of the integrated signal (see also sections 3.5 and 6.2.4). In Fig. 6.15 (right panel) the overshoot and the related undershoot of the SLOW signal are visible. This effect is most pronounced for small input amplitudes. Both problems could be solved by requiring a logical AND between the

delayed leading edge of the FAST and the leading edge of the SLOW signal as the release condition of the DISCHARGE signal implemented now as a Latch in the FPGA. As an additional benefit the threshold of the SLOW signal can now be set to very low relative threshold values. This is especially needed to gain the maximum in dynamic range. Even a threshold of the SLOW channel touching the noise, when the count-rate of the SLOW channels is higher than the count-rate of the FAST channels, is possible without releasing the DISCHARGE signal.

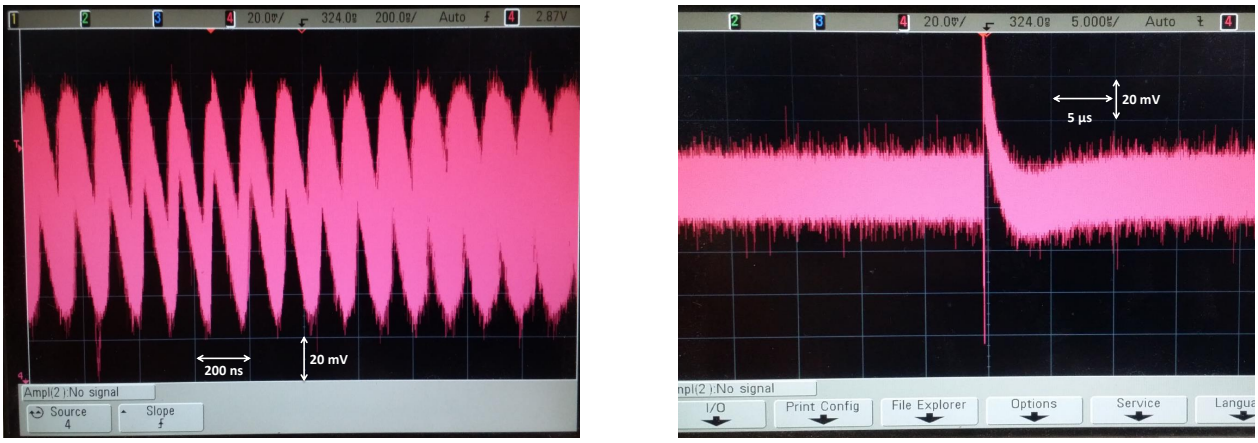


Figure 6.15: Left panel: Oscillation in the SLOW signals which starts for very low relative threshold values. The oscillation is caused by re-triggering on an undershoot which is related to the overshoot in the SLOW signal. **Right panel:** The undershoot is especially visible for small input signals. To avoid the re-triggering, the DISCHARGE signal must require the FAST signal which is not affected by re-triggering.

6.3.2 Adjustable Delay for starting the DISCHARGE Signal

The integration capacitors of the PaDiWa-AMPS board should ideally be discharged when the input pulse is fully integrated. This moment depends mainly on the width of the input pulse. Different pulse widths from different detector types need an adjustment for the start of the DISCHARGE signal. A delay, which is not synchronized to the FPGA clock, is needed in order to fit the width of the pulse. In the first version of PaDiWa-AMPS it was foreseen to generate the delay by routing the DISCHARGE signal out of the FPGA. A charging of a capacitance was foreseen outside the FPGA. When the threshold voltage of the input buffer is reached the signal is sent back inside the FPGA. By changing the size of the capacitance the charging time and therefore the delay can be changed. But laboratory test show that this principle cannot cover the required large delay range.

The new approach takes advantage of the fact that a signal which is routed inside the FPGA needs a specific time to pass through the electronic switches along its route. This causes a delay of the signal and is used to delay the DISCHARGE signal. For that the DISCHARGE signal is routed inside the FPGA along a defined path. In Fig. 6.16 the floor plan view of the FPGA is shown. It shows the placement of all instances which are used in the PadiWa-AMPS FPGA design. Two so called Stretchers are used to generate the delay. They have been placed in the lower left and lower right corner of the FPGA. Between both Strechers the DISCHARGE signal is routed back and forth. With the help of a Multiplexer it is possible to select the number of times the signal is routed between both Stretchers. In Fig. 6.17 the physical routing of all paths inside the FPGA is shown. In yellow the full signal path of the DISCHARGE signal is marked. Starting at the input pin the FAST signal is routed to an instance which generates the DISCHARGE signal. From there the DISCHARGE signal is routed between the two Stretchers back and forth. The Multiplexer which allows the selection of the implemented paths is then connected with the DISCHARGE output pin. From there the signal enters the analog part of the front-end board (see Fig. 2.4)

and finally discharges the integration capacitance. Currently the Multiplexer allows the selection of 16 repetitions through the Stretchers.

A single propagation through the Stretchers takes about 2 ns in each direction. The total delay can be adjusted between 18 ns and 65 ns. In Fig. 6.18 all possible delays between the FAST signal and the DISCHARGE signal are shown. The delays can be selected in real time via slow control of the PadiWa-AMPS board. For input pulse width below 18 ns it would be preferable to decrease the minimal delay time. This should be possible by adding a shortcut to the multiplexer.

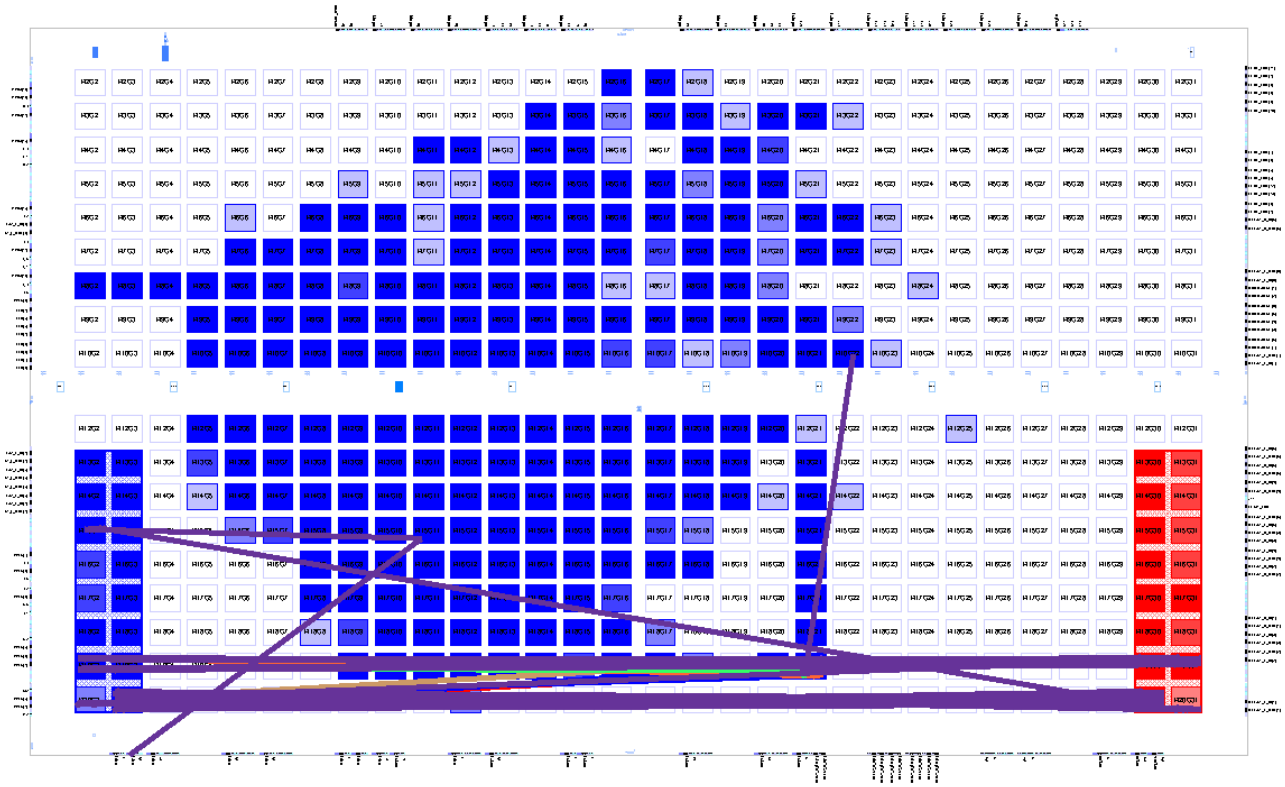


Figure 6.16: Floorplan view of the FPGA taken from the Lattice Diamond® Software. The stretchers are located in the left and right lower corners. The Magenta lines show the location of the instances which are needed to generate and delay the DISCHARGE signal.

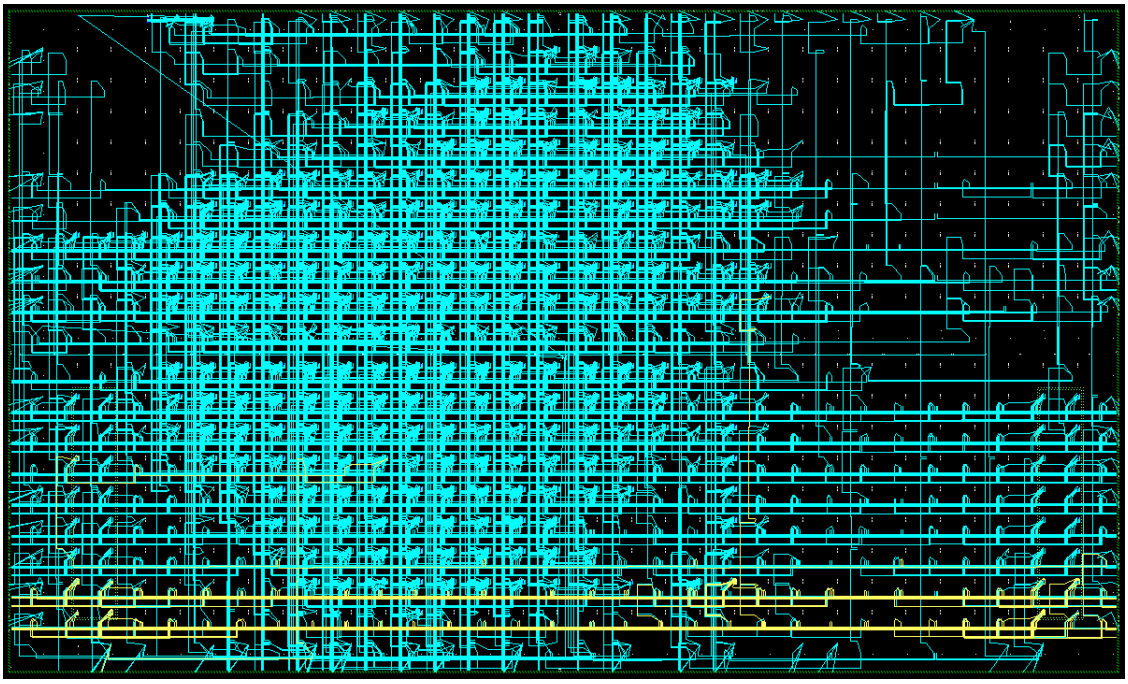


Figure 6.17: Physical view taken from the Lattice Diamond® Software. All paths inside the FPGA are shown in blue. The signal line of the DISCHARGE signal is shown in yellow. Starting at the FAST input, to the place where the DISCHARGE signal is generated. From there it is routed through the Stretcher and ends at the Multiplexer, which allows the selection of the delay. From the Multiplexer it is routed to the output pad.

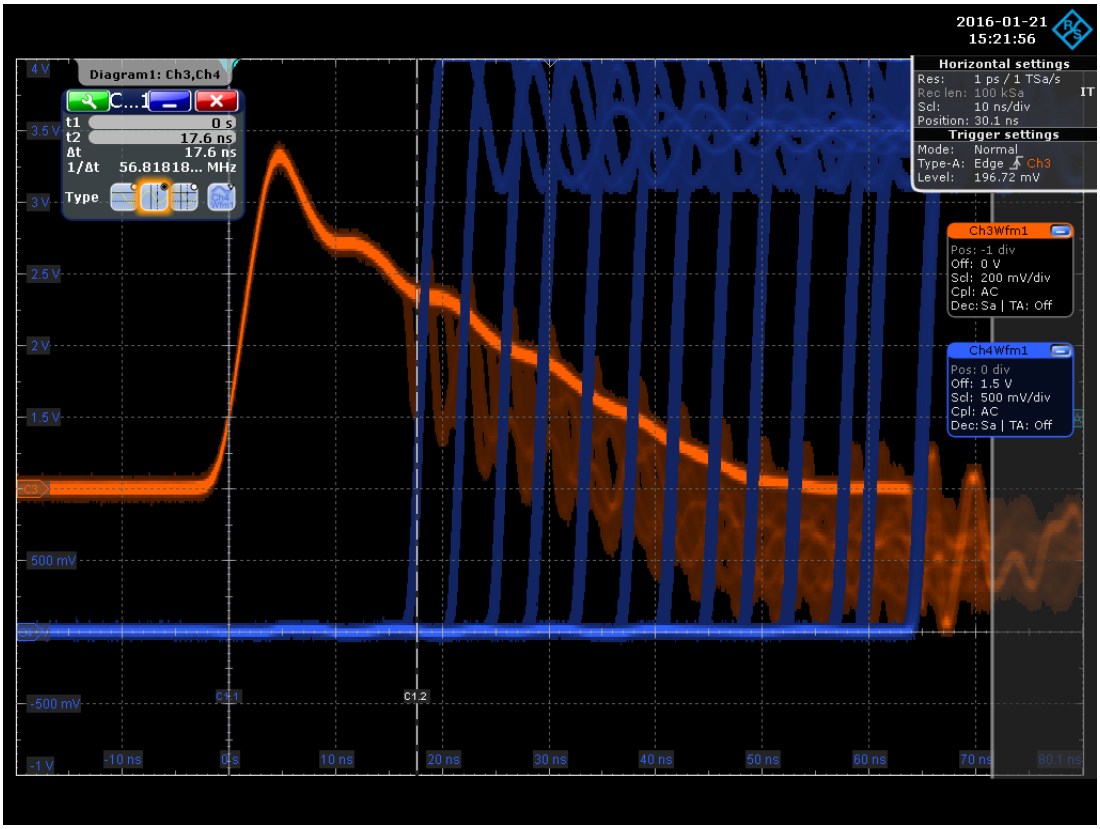


Figure 6.18: Selectable delays for the DISCHARGE signal are shown in blue. The FAST signal is shown in orange. Delays from 18 ns up to 65 ns can be selected in steps of about 4.5 n.

7 Summary and Outlook

The HADES experiment, which is located at GSI Helmholtzzentrum für Schwerionenforschung GmbH in Darmstadt, explores strongly interacting matter at high baryon chemical potentials ($\mu_B \geq 700$ MeV) and moderate temperatures ($T \leq 100$ MeV) using very rare and penetrating probes. With the realization of the FAIR (Facility for Antiproton and Ion Research) accelerator complex in Darmstadt, a new possibility will open to study the properties of matter in the vicinity of the first order phase transition and critical end point. The HADES and Compressed Baryonic Matter (CBM) experiments will be able to measure rare probes (dileptons, (multi-)strangeness and fluctuations of the conserved quantities) in the energy range where no data exist.

The upgrade of HADES with an electromagnetic calorimeter (ECAL) is planned for 2017-2018. This detector will allow to measure π^0 and η meson yields via their two photon decay channel. Also rare ω mesons could be accessible via their $\pi^+\pi^-\pi^0$ and $\pi^0\gamma$ decay channels. It would be possible to reconstruct direct photons and a variety of rare strange baryons. Furthermore, the ECAL will significantly improve the electron-to-pion separation at large momenta ($p > 400\,\mathrm{MeV/c}$). For CBM a Projectile Spectator Detector (PSD) is foreseen for determination of the collision centrality and orientation of the reaction plane. Both detectors (ECAL, PSD) will be read-out using the concept discussed in this work.

A Charge-to-Digital-Converter (QDC) and Time-to-Digital-Converter (TDC) based on an commercial FPGA (Field Programmable Gate Array) was developed to read out PMT signals of the planned HADES electromagnetic calorimeter (ECAL). The main idea is to convert the charge measurement of a detector signal into a time measurement, where the charge is encoded in the width of a digital pulse. The PaDiWa-AMPS front-end board for the TRB3 (General Purpose Trigger and Readout Board - version 3) which implements this conversion method was developed. The well-established TRB3 platform will take over the precise time measurement, which is also implemented in an FPGA, and serves as data acquisition.

The first PaDiWa-AMPS prototype front-end board was developed with the main purpose of the read-out of the HADES ECAL PMTs. The board showed good performance in the laboratory test. A time precision of 35 ps and a charge resolutions below 0.5% (for ECAL pulses > 1 V) was reached. The board was extensively tested in the laboratory and during beam times. SPICE simulations have been done to optimize the front-end in terms of charge and time resolution, dynamic range and signal-to-noise ratio.

In a beam time with secondary photons at the MAMI accelerator in Mainz the read-out concept was successfully used to read-out PMTs of HADES ECAL modules. It showed the same or even better precision in providing charge and time measurement than much more complex read-out systems.

During the HADES pion beam experiment the flexibility of the front-end was shown. The additionally installed Hodoscope detector was successfully read out by the PaDiWa-AMPS board. For that the analog part was adapted to the pulse shapes of small PMTs.

It is also planned to use the PaDiWa-AMPS board to read-out Si-PM signals of the CBM PSD detector. With the help of simulations and laboratory measurements it has been shown that an adjustment of the concept is possible. Challenging is the large dynamic range which has to be covered, in addition one has to deal with minimizing the external noise which is introduced by the Si-PM and it pre-amplifier. By optimizing the low and high frequency cut-off filters of the PaDiWa-AMPS board the signal-to-noise ratio could be significantly improved. Further improvements and tests are currently ongoing. A beam time test with the NA61/SHINE PSD detector at the CERN SPS is planned for the mid of 2016.

Furthermore, feasibility studies show that the read-out concept could be applied for diamond detectors. Further improvements regarding, in particular, the rate capability need an implementation of several features in the FPGA, i.e. the duration of the feedback signal depending on the area of the inte-

grator signal for an optimal baseline recovery. A redesign and manufacturing which implements all the optimization gained from this work is planned for the first half of this year.

8 Appendix

8.1 Field Programmable Gate Arrays - The Lattice MachXO2 Family

A field-programmable gate array (FPGA) is an integrated circuit which can be configured by a designer after manufacturing. It contains a large array of programmable logic blocks which represent mainly FlipFlops (FF) or Latches. In a modern FPGA up to several million logic blocks are implemented. So called Look-Up-Tables (LUTs) sum up a hand of logic blocs and contain several inputs and outputs. They can do any logical combinations (AND, NAND, XOR, Multiplexer etc.) out of the input signals. A routing matrix allows to "wire" the LUTs and therefore the logic blocks together. One LUT can do a little but with lots of connected LUTs complex logic functions can be created. The logic can be described by a hardware description language (HDL), for example VHDL or Verilog. At the boundary of the device I/O cells are implemented and arranged in so called banks. They are connected to the pins of the FPGAs, which allow it to communicate with the outside world. Here for example Low Voltage Differential Signaling (LVDS) is used. The TRB3 board, which is introduced in chapter 2, implements among others a high precision TDC implemented in a Lattice EPC3 FPGA. The "little brother" of an FPGA is a so called Programmable Logic Device (PLD). They have the same functionality as an FPGA but have a much simpler structure and provide about several thousand programmable logic blocks, less than an FPGA. The top level architecture of the LATTICE MachXO2-400HC PLD is shown in the block diagram in Fig. 8.1 (left panel). This type of PLD is used in the PaDiWa-AMPS prototype board, which is introduced in chapter 2. Inside this type of PLD discriminators are realized. The core of the MachXO2 device consists of so called Programmable Functional Unit (PFU) blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices as shown in Fig. 8.1 (right panel). Each slice contains two LUTs and two registers (Flip-Flops or Latches). In total there are 53 inputs and 25 outputs associated with each PFU block.

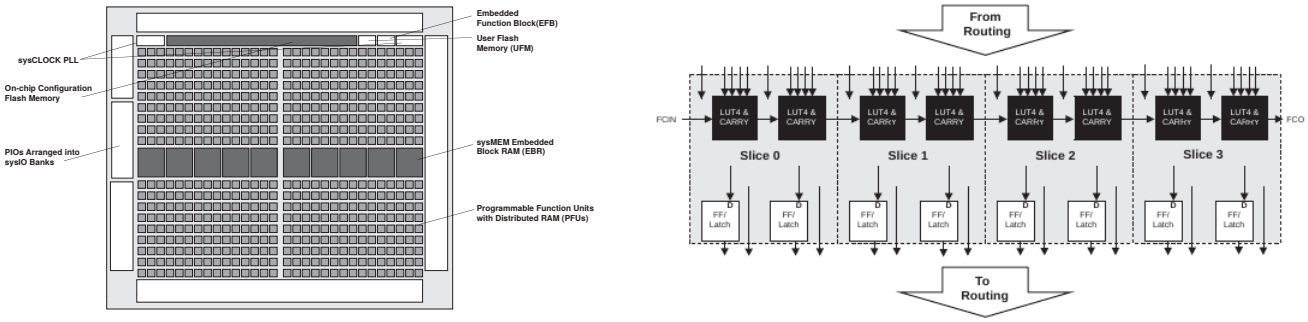


Figure 8.1: Left panel: Top-level architecture block diagram of the LATTICE MachXO2-4000HC PLD [35]. **Right panel:** A Programmable Functional Unit (PFU) block consists out of four interconnected slices. Each slice contains two LUTs and two registers (Flip-Flop or Latch). There are 53 inputs and 25 outputs associated with each PFU block [35].

8.2 PaDiWa-AMPS Control Software

The TRB3 and its front-end boards can be configured by a comprehensive software package, called trbsoft. Configuration commands can be send via command line and via a HTML based graphical user interface (GUI). The GUI is very lightweight and user friendly. Tool-tips support the operator by the configuration of the DAQ and CTS systems. The present settings and status information is shown in the GUI. The status of the DAQ is visualized and real-time rate plots are shown in a gnuplot plugin window. In Fig. 8.2 the GUI of the Central Trigger System is shown. Here the different trigger types can be selected. The screen-shot in Fig. 8.2 (right panel) shows the PaDiWa-AMPS slow control main page. Here channels can be enabled or the delay of the discharge signal can be set.

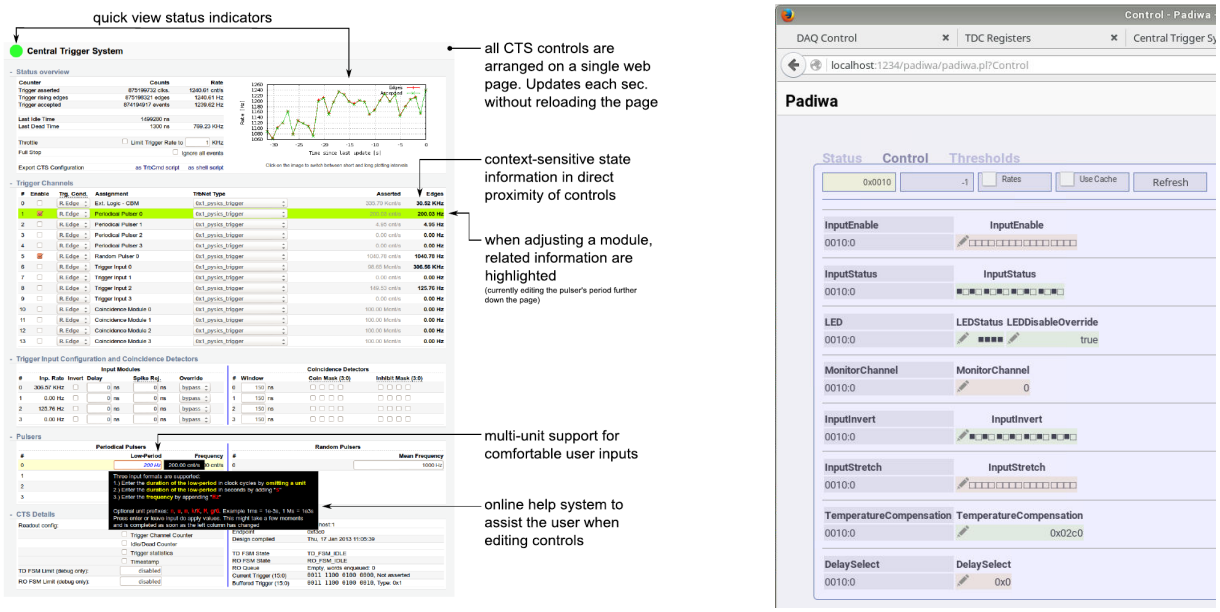


Figure 8.2: Left panel: Screen-shot of the HTML based CTS GUI. It shows the main page of the Central Trigger System [10]. **Right panel:** Screen-shot of the PaDiWa-AMPS slow control main page. Input channels can be enabled and the delay of the discharge signal can be set.

8.3 SPICE Simulation Software

For simulation of the response of analogue electronic circuits to input signals the so called SPICE (Simulation Program with Integrated Circuit Emphasis) analysis package is used. It solves numerically the differential equations for a given circuitry composed out of resistors, capacitors and inductors as well as diodes, transistors and more complex elements like operational amplifiers, delay lines or electronic switches. Diodes and transistors are described by a set of standard parametrized functions. The set of parameters is provided by the manufacturer of the component in a standardized way as so called SPICE models. More complex components are based on the basic elements mentioned before. The temperature dependence of the response function- in particular of diodes and transistors- is normally included in the models. In order to obtain reliable results, the parasitic elements like capacitance in parallel to a resistor or inductor (typically 0.2 pF) or inductance in series with a capacitor (typically 0.5 nH) should be included as 'virtual' components not explicitly mounted on a printed circuit board. They can play a significant role at high frequencies typically above 1 GHz. The values of these parasitic elements are normally provided by the manufacturer. For diodes and transistors the parasitic elements like inductance of bond wires and capacitance of solder pads are in general included in the SPICE models.

Various companies provide graphical user interfaces to allow the user to define the circuitry as well as providing graphs of the circuitry response to an input signal as function of time. Frequently used simulation packages are Pspice, Hspice, LTSpice, 5Spice, Tina or Multisim. Some of these products are freeware like LTSpice and the commercial tool 5Spice which have been used in this work. A simulation package for LTSpice can be found in [57].

8.4 Further Resources for the PaDiWa-AMPS Front-end and the TRB3-family

The full schematics of the PadiWa-AMPS front-end board can be accessed via the following web page. This web page is also a good starting point if one is looking for schematics of the TRB3 board and their AddOn and front-end bords like PaDiWa-AMPS. Beside this manuals can be found.

`http://trb.gsi.de/`

A user guide for the PaDiWa Front-Ends is currently being written and can be found in the following git repository:

```
git clone git://jspc29.x-matter.uni-frankfurt.de/projects/padiwadocu
```

The PaDiWa VHDL source code can be found the following git repository:

```
git clone git://jspc29.x-matter.uni-frankfurt.de/projects/padiwa
```

8.5 Optimized PaDiWa-AMPS Schematics of the Analog Part

Current optimized schematics of the analog part of PaDiWa-AMPS for the different detector types.

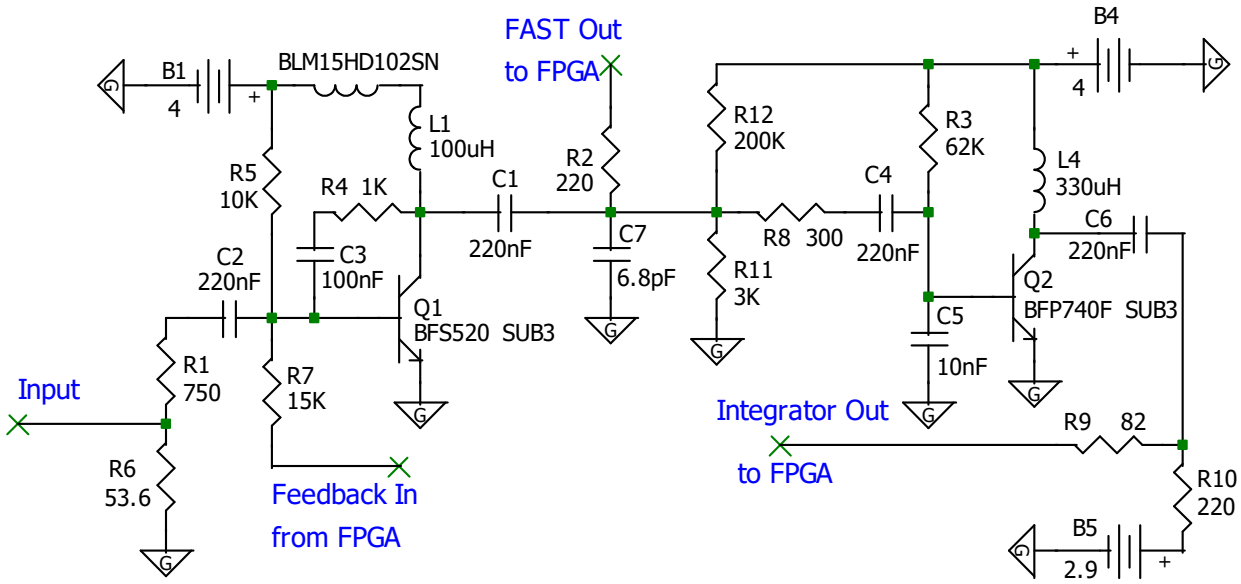


Figure 8.3: Current, optimized schematics of the analog part of PaDiWa-AMPS for HADES ECAL read-out.

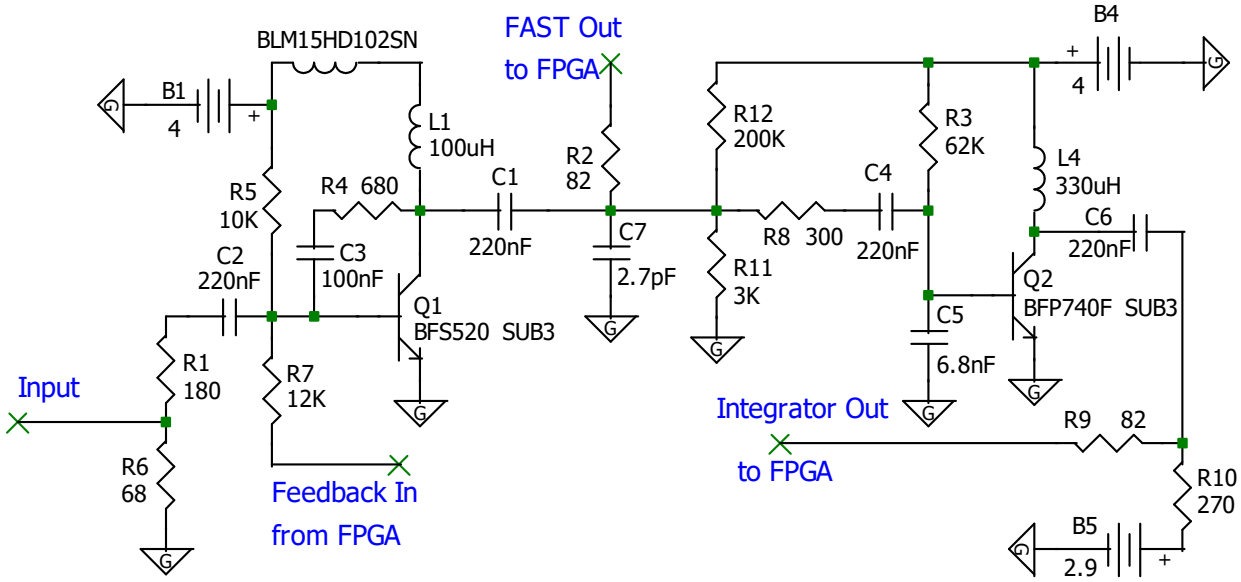


Figure 8.4: Current, optimized schematics of the analog part of PaDiWa-AMPS for HADES Hodoscope and Diamond Detector read-out.

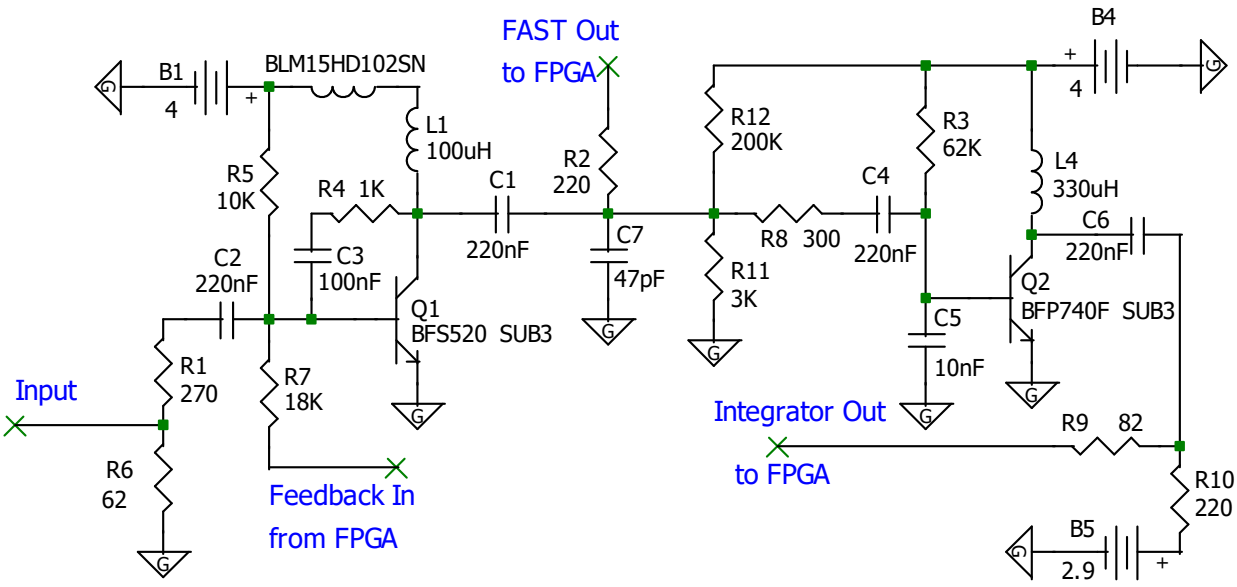


Figure 8.5: Current, optimized schematics of the analog part of PaDiWa-AMPS for Si-PM read-out.

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