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Design of an FPGA-based calibration, monitoring and testing system for the HADES Electromagnetic CALorimeter

Master of Science Thesis

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Contents

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Abstract

The High Acceptance DiElectron Spectrometer (HADES) at GSI (Darmstadt, Germany) was designed to measure dileptons in elementary and heavy ion collisions. An upgrade of HADES with an Electromagnetic Calorimeter (ECAL) has started and will be ready for beam in 2017. The goal is to measure π^0 and η yields together with the e^+e^- data in pion and proton-induced reactions as well as in heavy ion collisions. Moreover, photon measurement is important for neutral $\Lambda(1405)$ and $\Sigma(1385)$ spectroscopy. It is essential to precisely calibrate all the lead-glass crystal modules individually in order to achieve the required ECAL performances. Continuous monitoring and calibration with a light pulser system is required. It is foreseen to use blue light from an LED source, driven by short signals from a flexible pulse generator and distributed with optical fibers to each module of the ECAL. Due to their flexibility, Field Programmable Gate Arrays (FPGA) are chosen to implement the monitoring system. The signal produced by the FPGA can also be used, combined with some discrete electronics, to test the front-end board foreseen for the ECAL. The study, design and test of an FPGA-based pulse generator, as well as an hybrid (digital and analog) pulse generator are the main subjects in the thesis. Chapter 1 gives insight into the HADES experiment and its physics program. Chapter 2 is dedicated to calorimetry, with particular attention to the HADES ECAL. In addition, the read-out concept for this detector and the motivation for the calibration and monitoring system will be discussed. Chapter 3 collects some general remarks on FPGA-based implementations. In Chapter 4 and 5 the design of the pulse generators are thoroughly discussed. Finally, Chapter 6 is dedicated to the testing phase.

Chapter 1

Introduction

1.1 Physics Background

Over the last decades a lot of effort has been devoted to the study of nuclear matter far from its ground state. The goal of this initiative is to explore the phase structures of strongly interacting matter governed by the laws of Quantum-Chromo Dynamics (QCD) by creating new states of matter in the laboratory. Experiments studying heavy-ion collisions are the only possibility on earth to explore nuclear matter under conditions similar to those which appeared a few microseconds after the Big Bang, or as they still exist in the interior of compact stellar objects.
A qualitative picture of the phase diagram of nuclear matter as a function of temperature (T) and net baryon density (ρ_B) is shown in Figure 1.1. It is assumed that the matter present in the early universe at very high temperature (smaller than 200 MeV) about 10 μs after the Big Bang, while the universe cooled down, essentially traversed the phase diagram downwards, along the temperature axis. Compact stellar objects like neutron stars have zero temperature and exist in the region of high net baryon density. Nuclei exist at nuclear matter ground state density ($\rho_0 = 0.16$ fm^3) and at zero temperature. Nuclei are well-defined systems containing up to a few hundred nucleons held together by the nuclear forces. Nucleons, i.e. protons and neutrons comprise three valence quarks uud and ddu, respectively. In general, at low T and ρ_B, quarks and gluons are bound together (the so called confinement) to form colorless objects, called hadrons. As T and/or ρ_B increase hadrons

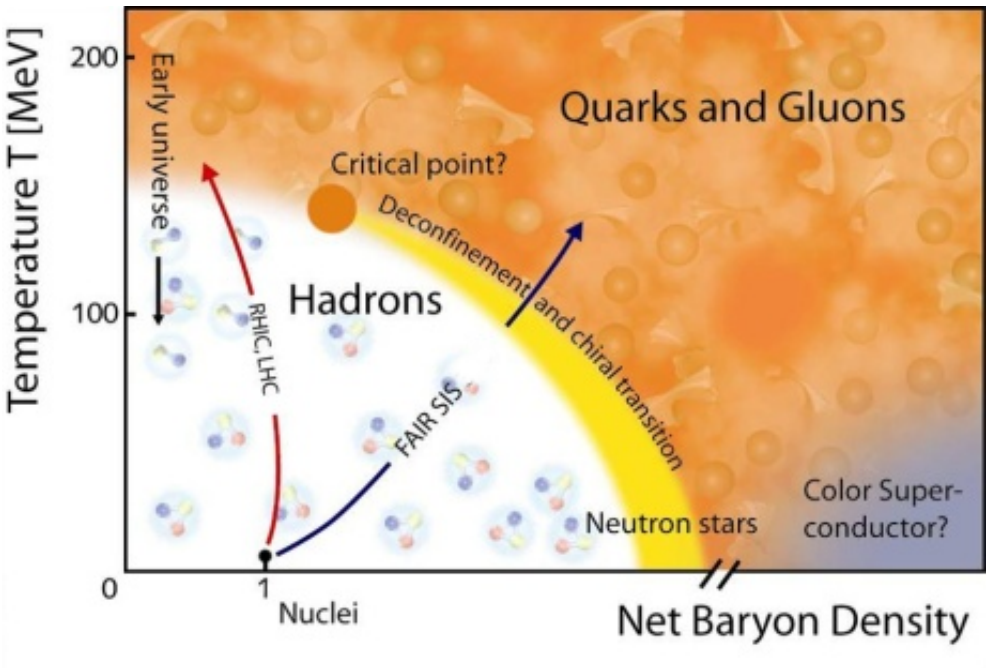

Figure 1.1: The phase diagram of QCD [1].

occupy more and more of the available space and thus start to overlap. The initially confined quarks and gluons separate creating new degrees of freedom other than hadronic ones. This deconfined phase is named Quark-Gluon Plasma (QGP) [2]. The present expectation is that the transition from the QGP to the hadronic phase is of first order in the region of large net baryon density. For a first order phase transition, a coexistent phase should exist where the phase is characterized by droplets of deconfined matter embedded in a gas of hadrons. Towards smaller net baryon density, the coexistence phase might terminate in a critical point having special and universal thermodynamic properties. At even smaller net baryon densities, lattice QCD predicts a smooth cross-over between the two phases. The possible new physics in the QCD phase diagram are Color Superconducting phases which might be important at asymptotically high baryon number density and low temperatures [3]. At finite temperature and density the existence of a new phase of QCD, Quarkyonic matter, has been suggested [4]. Quarkyonic matter is distinct from the confined and deconfined phases and represents the matter which is confined, yet chirally symmetric.

Current and future experiments at the RHIC, at the BNL and at the LHC at CERN energies concentrate on the study of matter in the regime of high temperatures and at very low net-baryon densities, i.e. in the region where a smooth crossover from a deconfined to hadronic phase is predicted by lattice QCD calculations. The accelerator facilities AGS at BNL and the SPS at CERN accessed extreme states of matter at still high temperature but at higher net-baryon densities. Probably, in this energy regime deconfined matter was created for the first time in heavy-ion collisions. At even lower beam energies, around 1 - 2 AGeV at the Bevalac and current GSI SIS18 facilities a large region in the nuclear matter phase diagram ranging from ground state matter density ρ_0 up to about 3 ρ_0 can be accessed with a proper choice of the collision system. The reaction volume is heated up to rather moderate temperatures (around 80 MeV) very likely without reaching the QGP phase boundary.

1.2 The HADES experiment

1.2.1 HADES physics program

HADES is a fixed target experiment currently operating on a beam line of SIS18 at GSI Helmholtzzentrum für Schwerionenforschung in Darmstadt, Germany. The location of the HADES cave is shown in Figure 1.2. At SIS18 the available energy range is up to 4.5 GeV for protons and 1.5 AGeV for heavier nuclei up to Gold. It is foreseen to move the detector in front of the CBM experiment [5], once the new FAIR facility will be completed. FAIR will feature a new synchrotron, SIS100 [6], which will enable to further accelerate protons up to 29 GeV and heavy nuclei up to 7 AGeV.

The main part of HADES physics program is focused on the study of the properties of dense baryonic matter at moderate temperatures via high resolution measurements of dielectrons and charged hadrons produced in elementary and heavy ion reactions, at beam energies of 1 - 3.5 AGeV. Spectroscopy of vector mesons like ρ, ω, ϕ is of particular interest for two main reasons: these particles are short-lived with lifetimes comparable, or even shorter than the duration of the compression phase of relativistic

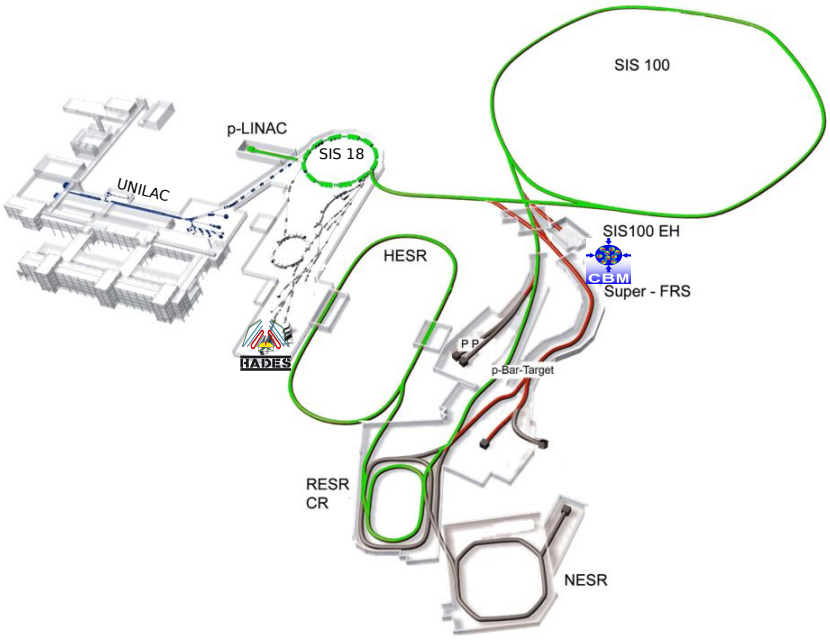

Figure 1.2: The existing GSI facility (grey) and the planned future facility FAIR (green and red) [6].

heavy-ion reactions in the SIS18 regime, and moreover their electromagnetic decay branch into e^+e^- pairs is not subject to strong final-state interaction and thus provides an undistorted signal of the early stages of the collision. Dilepton decay of vector mesons at SIS18 energies are rare events and their observation presents a challenge for the detector design. Detection of hadrons, not only the lightest ones like pions but also the ones containing the strange quark, like K, Λ, Σ, is possible with the HADES apparatus as well [7].

1.2.2 Detector overview

HADES features six identical sectors (see Figures 1.3 and 1.5) defined by the superconducting coils producing the toroidal geometry magnetic field. The momentum reconstruction is carried out by measuring the deflection angle of the particle trajectories derived from the hit positions in the four planes of Mini Drift Chambers (MDC) located in front of and behind the magnetic field region. The electron identification is performed with a hadron-blind gas Ring Imaging CHerenkov detec-

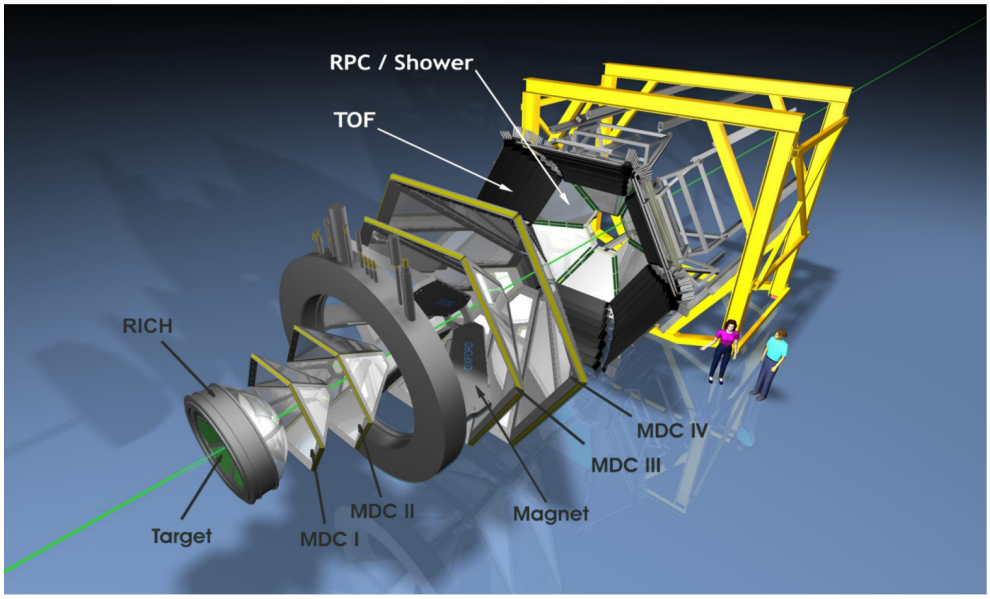

Figure 1.3: Expanded view of the HADES detector.

tor (RICH) together with the Multiplicity and Electron Trigger Array (META) consisting of Time-Of-Flight scintillator walls (TOF), Resistive Plate Chambers (RPC) and an electromagnetic Shower Detectors (Pre-Shower). A powerful trigger system employes diamond detectors (Start-VETO), respectively located upstream and downstream the target, and the META information to select events within a predefined charged particles multiplicity interval. At the very end, one meter downstream of the Pre-Shower detector, a Forward Wall is located. Its main goal is the detection of spectators, i.e. the nucleons which have not undergone interaction and thus followed a straight trajectory. The spectrometer has 85% azimuthal acceptance and covers polar angles between 18° and 88°. The reconstruction efficiency is approximately 90% for $p > 500$ MeV/c and the invariant mass resolution is around 15 MeV/c^2 [7].
For the future campaigns at SIS18 and later at SIS100, an upgrade of HADES foresees the replacement of the Pre-Shower detector with an Electromagnetic CALorimeter (ECAL). Most likely this upgrade will be completed already for the final run at SIS18 [8].

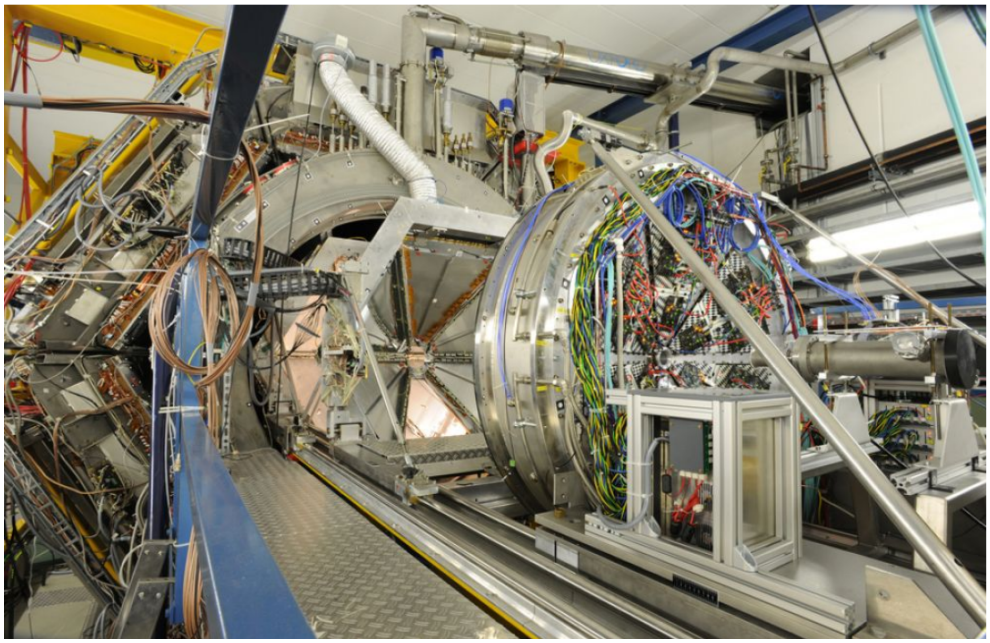

Figure 1.4: The HADES cave, front-view (in beam direction): the RICH detector (right) and the innermost MDC plane (left).

Figure 1.5: The HADES cave, back-view (in beam direction): Pre-Shower detector (right) and Forward Wall (left).

Chapter 2

The Electromagnetic CALorimeter for HADES

2.1 Calorimeters in high energy physics

2.1.1 General remarks and classification

The use of calorimetry in high energy physics is based on the idea of stopping an incoming particle in an absorber material, exploiting energy loss, and measuring its deposited energy. Calorimeters can be broadly divided into electromagnetic calorimeters, used to measure mainly electrons and photons through their electromagnetic interactions (e.g. bremsstrahlung, pair production), and hadronic calorimeters, used to measure mainly hadrons through their strong interactions. They can be further classified according to their construction technique into sampling calorimeters and homogeneous calorimeters. Sampling calorimeters consist of alternating layers of an absorber, a dense material used to degrade the energy of the incident particle, and an active medium that provides the detectable signal. Homogeneous calorimeters, on the other hand, are built of only one type of material that performs both tasks: energy degradation and signal generation [9]. The detection is based on the measurement of scintillation light (i.e. scintillator crystals, liquid noble gases), ionization (i.e. liquid noble gases) or the measurement of Cherenkov radiation (i.e. lead glass). The signal produced in the detection material is proportional to the deposited energy of the incoming particle. A very important parameter of

a calorimeter is its energy resolution, defined as

$$\frac{\sigma_E}{E} = \frac{a}{\sqrt{E}} \oplus \frac{b}{E} \oplus c$$

where the symbol $\oplus$ indicates a quadratic sum. The first term on the right-hand side is called the stochastic term, and includes the shower intrinsic fluctuations. The second term is called noise term. It comes from the electronic noise of the readout chain and depends on the detector technique and on the features of the read-out circuit, e.g. detector capacitance and cables. The third term is the constant term and includes contributions which do not depend on the energy of the particle. Instrumental effects that cause variations of the calorimeter response with the particle impact point on the detector give rise to response non-uniformities. The relative importance of the various terms depends on the energy of the incident particle.

Since the HADES ECAL will be a homogeneous electromagnetic calorimeter based on the detection of Cherenkov radiation, hereafter the interest will be addressed exclusively on this kind of detectors.

2.1.2 Theory of electromagnetic calorimeters: the Rossi-Heitler model

The Rossi-Heitler is a simplified model that allows to describe the development of an electromagnetic shower [10]. This latter starts when either a photon or an electron/positron with energy above a few MeV interacts with a medium, producing a cascade of secondary particles with lesser energy. In the high energy regime, photons interact with matter primarily via e^+ - e^- pair production and electrons/positrons primarily via photon emission in a bremsstrahlung process. The model keeps into account only these two interaction processes to account for the energy loss of the particles. The parameter that characterizes the development of the electromagnetic shower is the radiation length

$$X_0\,(\mathrm{g/cm^2}) \simeq \frac{716\,\mathrm{g/cm^2}\,A}{Z(Z+1)\,ln\,(287/\sqrt{Z})}$$

where Z and A are the atomic number and weight of the material, respectively. X_0 represents both the mean distance over which a high energy electron loses $1/e$ of its energy by bremsstrahlung and approximately the mean free path for pair production by a high energy photon (in the formula there is a numerical factor 7/9 that can be approximated to unity in this modelization). A convenient measure to consider for the shower longitudinal development is the distance normalised in radiation lengths: $t = x/X_0$. After one radiation length the photon produces an e^+ - e^- pair; electrons and positrons emit after another radiation length one bremsstrahlung photon each, which again are converted into e^+ - e^- pairs. Assuming that the energy is symmetrically shared between the particles at each step of the multiplication, the number of shower particles (electrons, positrons and photons together) at depth t is

$$N(t) = 2^t$$

The energy of the individual particles at t is given by

$$E(t) = E_0/N(t) = E_0 \cdot 2^{-t}$$

The multiplication of the shower particles continues as long as E_0/N is bigger then a critical energy E_c. The critical energy can be defined as the energy at which the electron ionization losses and bremsstrahlung losses become equal, or as the energy at which the ionization loss per X_0 equals the electron energy [10] [11]. The position of the shower maximum is reached at this step of multiplication, i.e. when

$$E_c = E_0 \cdot 2^{-t_{max}}$$

This leads to a maximum depth

$$t_{max} = \frac{ln\,(E_0/E_c)}{ln\,2}$$

The corresponding number of particles present in the shower is

$$N(t_{max}) = E_0/E_c = 2^{t_{max}}$$

The logarithmic dependence of t_{max} on E_0/E_c is a great advantage, for a relatively small thickness (around 10 - 15 X_0) is sufficient to stop a

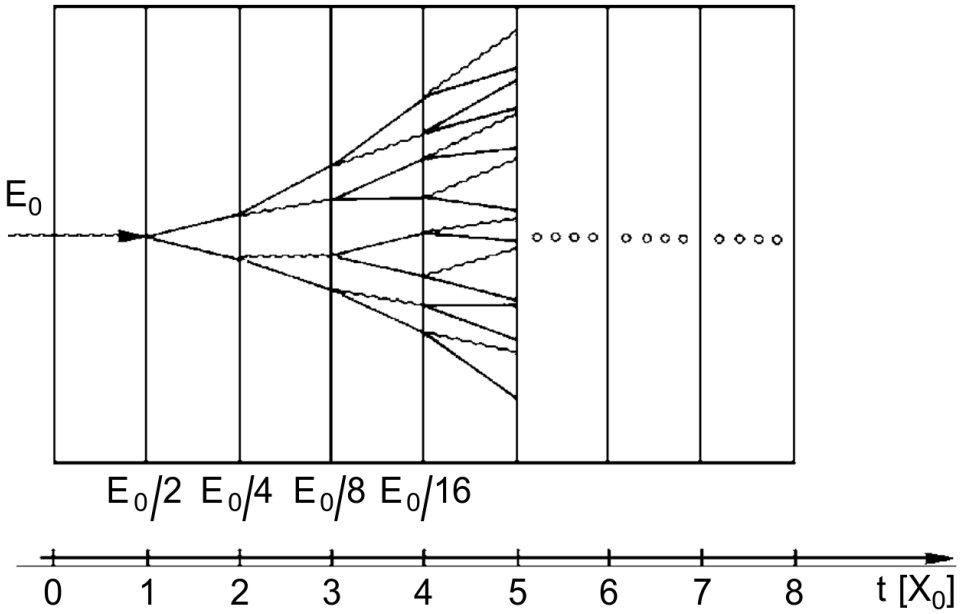

Figure 2.1: Sketch of a simple model for shower parametrisation: the wavy lines are photons and the solid lines electrons or positrons [10].

high energy particle. Figure 2.1 shows a schematic view of an electromagnetic shower. The angular distribution of the particles produced by bremsstrahlung and pair production is very narrow. Thus the lateral width of an electromagnetic cascade is mainly determined by multiple scattering and can be best characterised by the Molière radius

$$R_M = \frac{21\,\mathrm{MeV}}{E_c} X_0 \ [\mathrm{g/cm^2}]$$

Generally speaking, about 95% of the shower energy is contained in a cylinder around the shower axis whose radius is $R(95\%) = 2R_M$. This containment radius is almost independent on the energy of the incident particle but exhibits a strong dependence on the material, through the critical energy and radiation length appearing in the definition.

2.1.3 Homogeneous Cherenkov calorimeters

The main advantage of homogeneous calorimeters is their excellent energy resolution, which is due to the fact that the whole energy of an incident particle is deposited in the active medium, in contrast with sampling

calorimeters. On the other hand, homogeneous calorimeters can be less easily segmented laterally and longitudinally, which is a drawback when position measurements and particle identification are needed.
Detectable Cherenkov light is produced whenever a particle traverses a transparent medium with a speed $v > c/n$, where c/n is the speed of light in that medium and n the refractive index of the medium. The photons from the active volume are converted into electrons, usually called photoelectrons, by a photosensitive device such as a PMT. Cherenkov light is emitted on the surface of a cone centered on the particle trajectory and with half angle $\theta_c = \arccos(c/nv)$. Dielectric materials with $n > 1$ are good candidates for Cherenkov detectors. In Cherenkov calorimeters the Cherenkov photons are produced by the relativistic $e^{\pm}$ showers. This kind of calorimeters usually have a worse energy resolution than other types of homogeneous calorimeters. This is mainly due to the fact that the light yield is small, usually 104 times smaller than in a scintillator, because only shower tracks with $v > c/n$ produce a detectable signal. In addition, the maximum photon intensity is obtained for short wavelengths, typically $<$ 300 - 350 nm, whereas most PMTs are sensitive to the region 300 - 600 nm. As an example, about 1000 photoelectrons are produced in lead glass per deposited GeV, which alone (i.e. without taking into account possible inefficiencies in the signal collection and other effects like shower containment) gives an energy resolution of approximately $3\%/\sqrt{E(\mathrm{GeV})}$.

2.2 ECAL in HADES

2.2.1 Motivations and goals

The deepest motivation for the introduction of an electromagnetic calorimeter in the HADES apparatus is the requirement of an exact knowledge of the physics background (e.g. e^+e^- pairs from π^0 and η decays), in order to perform precise dilepton measurements [12]. For the SIS18 energy range, production of the π^0 and η mesons has been studied extensively in heavy ion collisions by the TAPS collaboration via two photon calorimetry [13] and in N-N collisions by various detectors at Uppsala, Saclay and COSY

[14]. However, no specific data are presently available for the energy range 4 - 40 AGeV, with the consequence that any interpretation of future dielectron data would have to depend solely on theoretical models, e.g. transport model calculations or statistical hadronization models [15] [16] [17]. The ECAL will enlarge the experimental capabilities of the HADES spectrometer by allowing photon detection, not possible in the current set-up. Of particular interest is the measurement of π^0 and η meson yields via their two photon decay as well as the reconstruction of ω via the decay channel $\omega \rightarrow \pi^0\pi^+\pi^-$ and $\omega \rightarrow \pi^0 e^+ e^-$, which can be performed combining the two photon detection in the ECAL with a charged particle detected in the rest of the HADES spectrometer. Detection of direct photons and photons coming from decays of strangeness containing baryons, such as neutral $\Lambda(1405)$ and $\Sigma(1385)$ resonances, will be performed. Last but not least, an important bonus offered by the planned ECAL is the improvement of the electron/pion separation at momenta larger than 400 MeV/c.

2.2.2 ECAL properties and layout

The ECAL will be a homogeneous calorimeter based on the detection of Cherenkov light. It will consist of 978 modules on loan from the OPAL end-cap electromagnetic calorimeter experiment at CERN, divided into six trapezoidal sectors, same as the HADES setup. The energy resolution reported by the OPAL collaboration is

$$\frac{\sigma_E}{E} = \frac{5\%}{\sqrt{E[\mathrm{GeV}]}}$$

However, after several years of operation in a high radiation environment this value needs to be checked again. Lead glass CEREN 25 is used as a Cherenkov radiator. This lead glass has a density of 4.06 g/cm^3, a refractive index of 1.708 (at 410 nm), a radiation length of 2.51 cm and a Molière radius of 3.6 cm. The light transmission coefficient for this lead glass length is about 0.96 at 400 nm. Each lead glass block is 420 mm long and has transverse dimensions of 92 x 92 mm^2, comparable to the transverse size of the electromagnetic showers, and will be equipped with its own PMT (see Figure 2.2). The lead glass block is

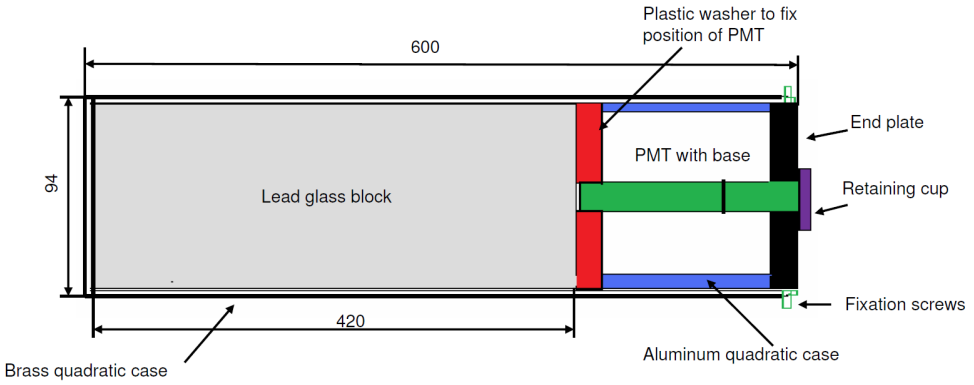

Figure 2.2: Schematic view of the calorimeter module.

housed in a brass can. The wall thickness of the can is 0.45 mm. All surfaces of the lead glass blocks are mirror polished. All sides of the block, except the end to which the PMT is attached, are wrapped with white paper (Tyvek®). Studies confirmed that this reflector in combination with the optical grease (Rhodorsil® Paste N. 7) between PMT and lead glass improves the energy resolution by about 10% in comparison with aluminum or mylar reflector materials. The position of the PMT on the rear side of the lead glass block is fixed by a plastic plate with a hole at the center. The PMT, together with its high voltage divider, is fixed by a retaining cup on the end plate. The end plate is connected to the aluminum can ensuring that the mechanical structure of the module is more rigid. The can provides the mechanical support of the assembly via the end plate which is secured by a rigid back plate. The reflective foil, the brass can and the space between the counters add additionally 2 mm in the transverse direction. Therefore, the counters are mounted on a 94 mm pitch. The components of the calorimeter modules are shown in Figure 2.3.

As already mentioned, the ECAL will replace the currently used Pre-Shower detector. It will cover the area of 8 m^2 corresponding to a polar angle coverage between 12° and 45° and almost full azimuthal angle coverage, except the slots between the sectors, matching the geometrical acceptance of the full spectrometer. Each sector will include 15 rows of modules. The mass of each module is approximately 15 kg that leads

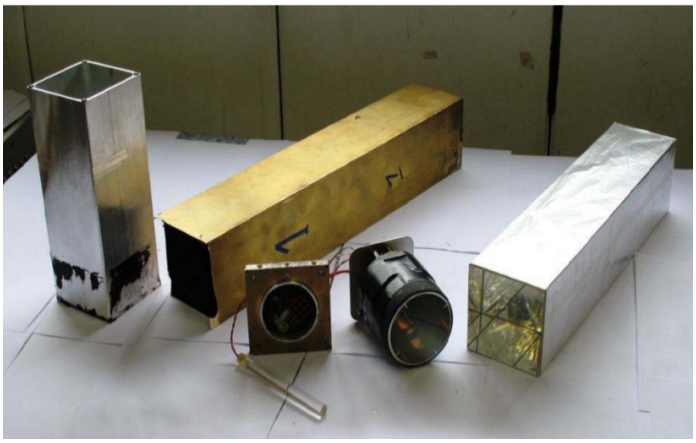

Figure 2.3: A disassembled ECAL module: the brass housing (left), the lead glass block (right), the high voltage divider and the PMT (middle).

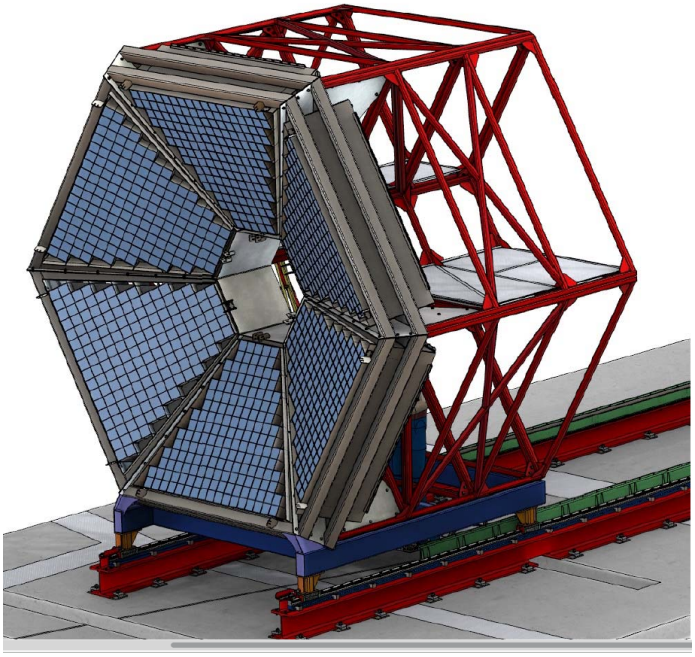

Figure 2.4: 3D model of the ECAL mounted on its support structure.

to an overall mass of about 15 tons. A dedicated mechanical support structure has been designed to accommodate all the modules leaving the possibility of substituting a single module without large effort. The calorimeter will be placed on rails using ball-bearing based guidance, and it will be possible to displace it along the axis of the beam, to allow for access to the other detectors (Figure 2.4).

2.3 Read-out electronics

The duty of the read-out chain for the ECAL is basically to provide time and charge information of raw data coming from the detector. The read-out requirements are based on the following parameters, assumed for the ECAL PMT signals:

- rise time: 3 ns
- falling time: 50 ns
- S/N ratio: > 12.5
- pulse amplitude (20 MeV): 50 mV
- pulse amplitude (600 MeV): 1.5 V

The mentioned requirement are thus:

- time resolution: < 500 ps
- dynamic range of signal amplitude (energy): 100, so 50 mV - 5V
- accuracy needed for the energy measurement: $< 1\%$ at high amplitudes

Each calorimeter sector will deliver 163 independent signals for a total of 978 signals. The expected hit rate is 10 kHz per channel [8].
The idea behind the read-out electronics for the ECAL is to reuse elements which have been already successfully tested and are currently operating in the HADES set-up. The scheme follows the COME & KISS concept: use COMmercial Elements and Keep It Small and Simple [18]. In fact, instead of expensive application-dependent electronics (i.e. ASICs), common off-the-shelf components like flexible FPGA-based platforms, accompanied by further simple electronics circuits are used. The read-out chain can be split into three main parts, namely: the front-end board, the digitizing board and the data acquisition system (DAQ) [8].

2.3.1 The front-end board: PADIWA AMPS

The front-end board PADIWA AMPS (see Figure 2.5) is a modified version of the already existing PADIWA board. It provides 8 input channels that generate 16 signals. For each of these signals both edges can be measured. The board features a charge precision of 0.2% and a high dynamic range of 250. It uses the concept of a readout via a charge-to-width (Q2W) conversion based on FPGA (see 2.3.4) [19].

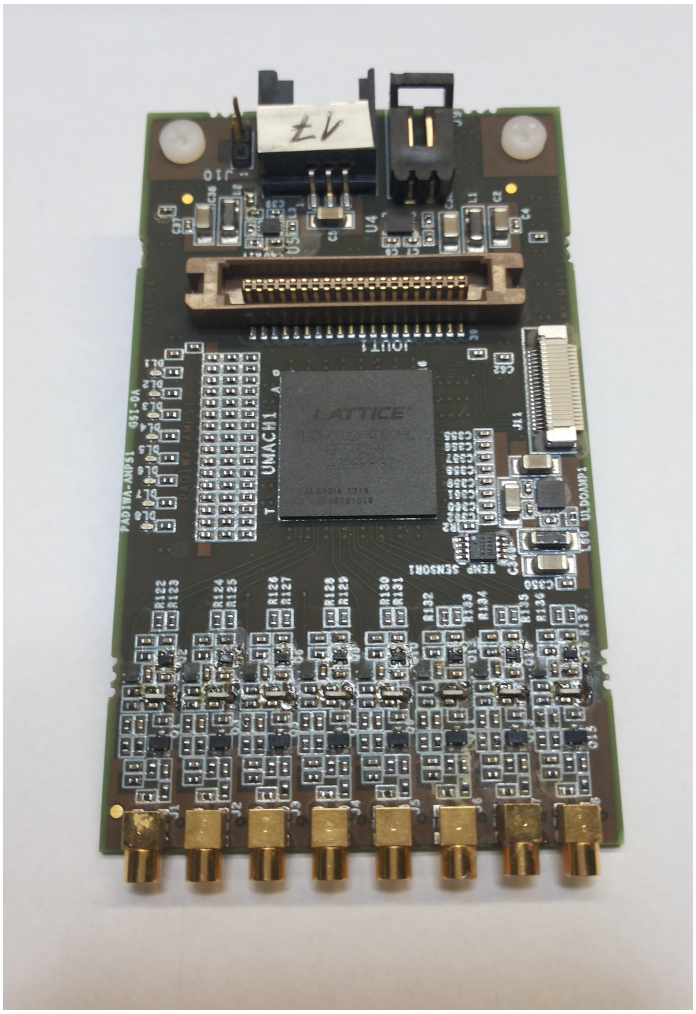

Figure 2.5: The PADIWA AMPS front-end board.

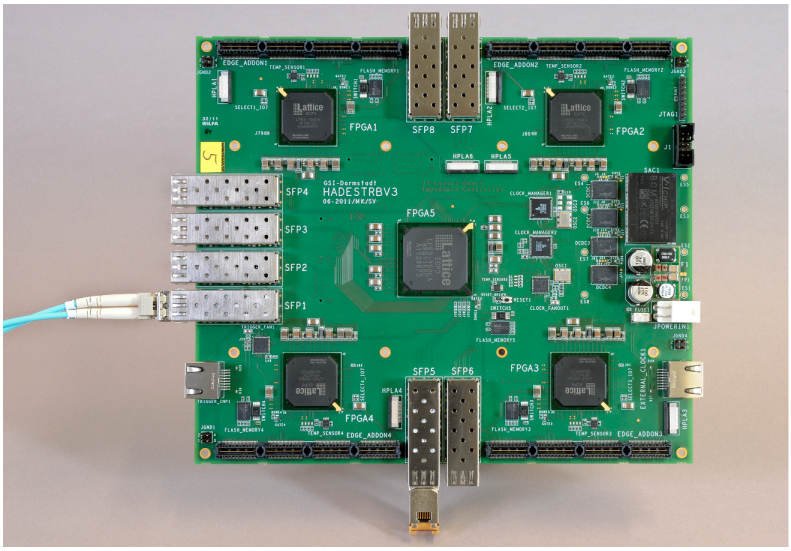

Figure 2.6: The Trigger and Read-out Board version 3.

2.3.2 The digitizing board: TRB3

The multipurpose Trigger and Readout Board version 3 (TRB3) (Figure 2.6) developed for HADES, PANDA (Barrel/Disk-DIRC and Straws) and CBM (RICH, MVD read-out) is the digitizing board foreseen for the ECAL [19]. An FPGA-based TDC with high rate, multi-hit and superior performance in terms of time precision (less than 20 ps RMS between two channels) allows the time measurement. The board also provides a high bandwidth DAQ functionality with data transfer capabilities up to several hundred MByte/s and can serve up to 256 detector channels. The digitizing board controls the parameters set on the front-end boards by separate slow control lines.

2.3.3 The data aquisition system

After digitizing, the data are combined to HADES-sub-events and sent to the HADES-DAQ network consisting of two parts: an FPGA-based custom network with optical links inside the detector and a commercial Gigabit Ethernet infrastructure to the server farm. The optical network features high bandwidth, low latency bi-directional data transport. All data are transported via this network on dedicated virtual channels: trigger information, event data and slow-control information.

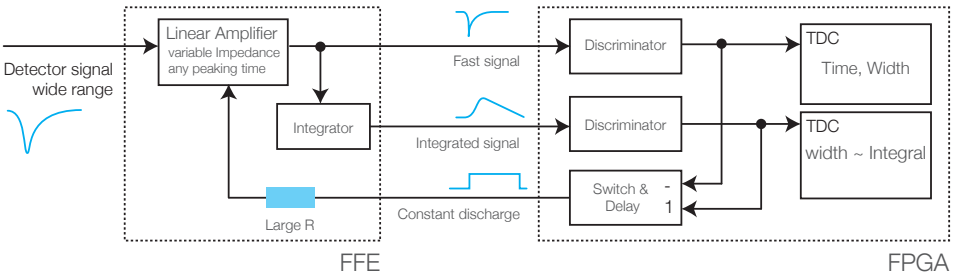

Figure 2.7: Sketch of the read-out system proposed for the ECAL. Signals after amplification are processed in the charge to width conversion system followed by the time digitization circuit which consists of two branches, one for fast timing and the second one for a pulse-width measurement which encodes the charge. Thus, two TDC channels are needed for one detector input channel.

2.3.4 The COME & KISS read-out

The signal processing consists basically of two parallel paths. The first one is the so called fast signal: it is an amplified version of the raw signal coming from the PMT (amplification factor of 0.5 - 5) and it preserves timing information of the rising and falling edges. The second one is the slow signal: the raw signal is integrated over a capacitor, which is subsequently discharged via a current source. The FPGA-based TDC is used to measure the discharge time, which is proportional to the integrated charge. Using the current source for the discharge results in a fast crossing of the threshold and therefore a better precision of the charge measurement is reached as compared to a RC-discharge method. In addition, the method of discharging the capacitor by applying a constant current over a time interval until the pulse charge is fully compensated works as an automatic baseline restorer. In fact for the integration accuracy it is important to keep the baseline rather constant. Furthermore, after discharging the integrator, the device is nearly immediately ready to process the next signal, i.e. low dead time of the channels. See Figure 2.7 for a schematic view of the read-out concept.

2.4 Calibration and monitoring system

2.4.1 General remarks

The pulse height A_i, measured in the i-th module, is related to the deposited energy E_i by

$$E_i = \alpha_i(A_i - P_i)$$

where P_i is the pedestal, i.e. the origin of the scale, and α_i is the calibration coefficient. Thus, to keep a good performance of the calorimeter, the following procedures are usually carried out:

- pedestal determination by providing a trigger from a pulser without any signal at the input (usually called *random trigger events*)
- electronics channel control by test pulses applied to the input of the electronics chain
- monitoring of the stability of the calibration coefficients α_i
- absolute energy calibration, i.e. determination of the α_i values

In general, the dependence can be non-linear. In this case, more calibration coefficients are needed to describe the energy-amplitude relation. Prior to real physics experiments a study of the parameters of individual calorimeter elements and modules is usually done during test beams which supply identified particles of known momenta. By varying the beam energy the linearity of the calorimeter can be tested and characteristic shower parameters can be recorded. Big experiments can contain a large number of calorimeter modules, not all of which can be calibrated in test beams. If some of the modules are calibrated in a test beam, the rest can be adjusted relative to them. This relative calibration can be done by using minimum-ionising muons that penetrate many calorimeter modules.
In calorimeters where the signal is collected in the form of light (e.g. Cherenkov calorimeters) it is common to perform calibration by feeding defined light signals, e.g. via LEDs, into the detector and recording the output signals from the PMTs. To avoid variations in the injected light

intensity, which may be caused by different light yields of the individual LEDs, a single light source and a manifold of light fibres to distribute its light can be used. Once a complex calorimeter system has been calibrated, it is important to ensure that the calibration constants do not vary or, if they do, the drift of the calibration parameters must be monitored. The time stability of the calibration can be checked, for example, with muons from cosmics rays. In some cases the calorimeter modules may be positioned unfavourably so that the rate of cosmic muons is insufficient for accurate stability control. Or they can be even isolated from cosmics during data taking. Therefore, reference measurements have to be performed periodically by injecting calibrated reference signals into the various modules or into the inputs of the readout electronics.

2.4.2 Calibration and monitoring of the ECAL

As already mentioned in 2.2.2, the final version of the ECAL will consist of around 1000 modules. It is necessary to test each module individually. Therefore a dedicated light pulse system for gain stability monitoring of the modules is foreseen [12]. The system is planned to be used both for initial testing of new modules as well as periodically during data taking to check the quality, time stability and thus accuracy of the detector. It is foreseen to use blue light from an LED source and an optical distribution system with optical fibers to transport the light to each module. Optical fibers will be equipped with a connector plugged on the cap at the end plate of each module, so that each module can be disconnected or replaced. These test light sources have to be driven by a short signal from a flexible pulse generator. Amplitude and width of the LED light pulses will be set to generate the same output from the detector as from the cosmic muons signals used for calibration.
In Chapter 4 the design and implementation of the mentioned flexible pulse generator will be shown in details.

Chapter 3

FPGA: Field Programmable Gate Array

It was decided to implement the mentioned pulse generator (see 2.4.1) on an FPGA platform. FPGAs offer several advantages with respect to discrete logic, e.g. they are off the shelf, have relatively low cost, are reconfigurable and fast, but the main reason for this choice is related to the intrinsic flexibility of FPGA designs.
In this chapter a short overview on FPGAs architecture and designs will be given.

3.1 FPGA architecture

An FPGA is an integrated circuit designed to be configured after manufacturing [20]. The most common FPGA architecture consists of an array of programmable logic blocks that provide the basic logic and storage functionality for a target application design, reconfigurable interconnections or routing channels that allow them to communicate and input/output connections for communication with the outside world (see Figure 3.1). In the simplest configuration a logic block consists of a look-up table (LUT) and a flip-flop. A LUT with k inputs (k-LUT) contains 2^k configuration bits and it can implement any k-input boolean function. Figure 3.2 shows a basic logic block comprising of a 4 input LUT (4-LUT) and a D-type flip-flop. The 4-LUT uses 16 bits to implement any 4 inputs boolean function. The output of the 4-LUT is connected to

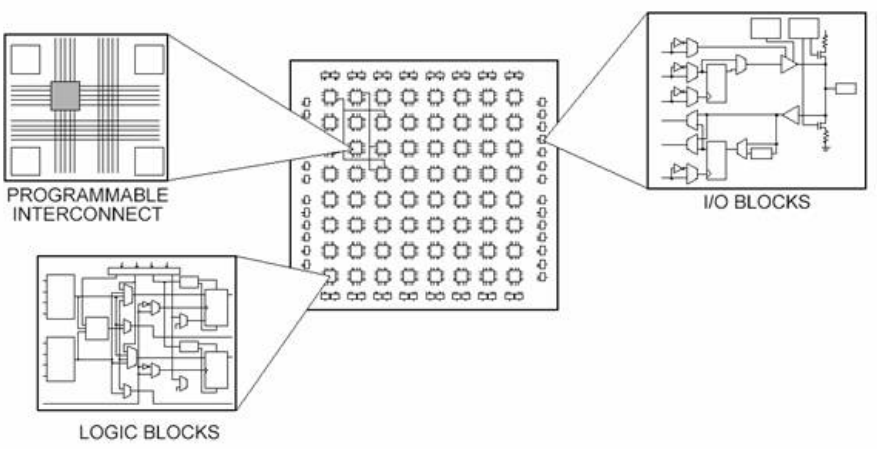

Figure 3.1: Basic scheme of an FPGA.

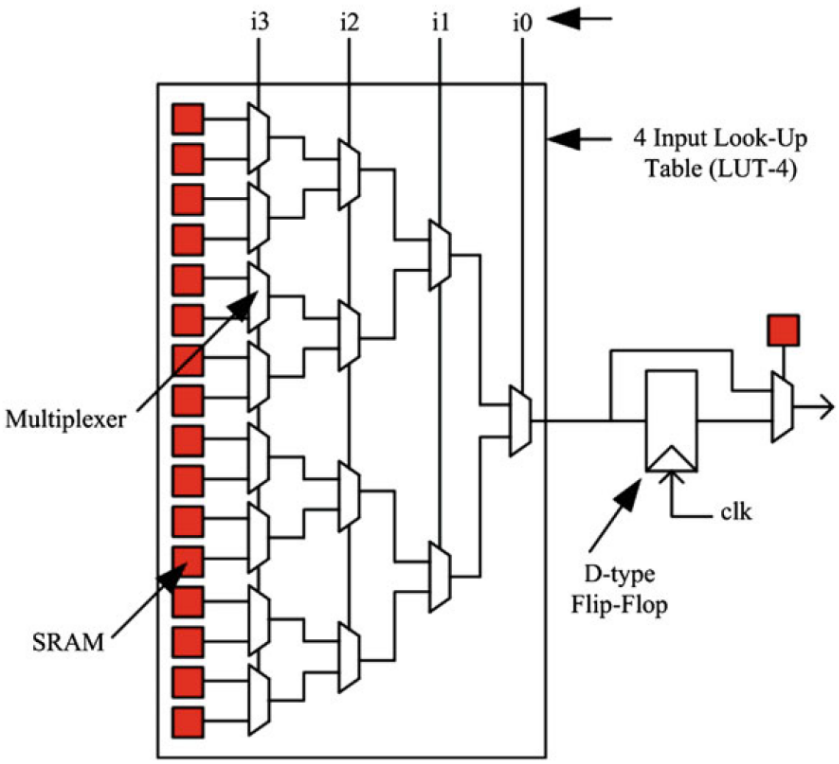

Figure 3.2: Basic logic element in an FPGA [20].

an optional flip-flop. A multiplexer selects the output to be either the output of the flip-flop or the 4-LUT.

The flexibility of an FPGA is mainly dependent on its programmable routing network. Since FPGA architectures should allow the implemen-

tation of any digital circuit, their routing interconnect must be very flexible so that they can accommodate a wide variety of circuits with widely varying routing demands. The routing interconnect of an FPGA consists of wires and programmable switches. Although the routing requirements vary from circuit to circuit, certain common characteristics of these circuits can be used to optimally design the routing of FPGA architectures. For example most of the designs exhibit locality, hence requiring abundant short wires. But at the same time there are some distant connections, which leads to the need for sparse long wires.
Most of the circuitry built inside an FPGA is synchronous circuitry that requires a reference signal, called clock signal. FPGAs contain dedicated global and regional routing networks for clock and reset so they can be delivered with minimal skew[1]. FPGAs generally contain also memory blocks like RAM, DSP slices and serializers. Moreover, analog PLL and/or DLL components are implemented to synthesize new clock frequencies. Complex designs can use multiple clocks with different frequency and phase relationships, each forming separate clock domains. These clock signals can be generated locally by an oscillator or they can be recovered from a high speed serial data stream.

3.2 FPGA design flow

A major aspect of FPGA architecture research is the development of CAD tools for mapping applications to FPGAs. It is well established that the quality of an FPGA-based implementation is largely determined by the effectiveness of accompanying suite of CAD tools. Benefits of an otherwise well designed, feature rich FPGA architecture might be impaired if the CAD tools cannot take advantage of the features that the FPGA provides. Thus, CAD algorithm research is essential to the necessary architectural advancement to narrow the performance gaps between FPGAs and other computational devices like ASICs.
The software flow (CAD flow) takes an application design description in

[1]Skew is defined as the time difference between two or more destination pins in a path.

a Hardware Description Language (HDL) and converts it to a stream of bits that is subsequently programmed on the FPGA. The process of designing and converting a circuit description into a format that can be loaded into an FPGA can be roughly divided into several steps, namely: circuit design and simulation, logic synthesis, technology mapping, placement and routing, timing analysis and bitstream generation.

Circuit design and simulation

The first step in the implementation of a circuit on an FPGA platform is the design of the circuit itself. The developer can choose among several Hardware Description Languages, e.g. VHDL and VERILOG. In the following, attention will be addressed to VHDL since this is the language used to design the mentioned pulse generator. VHDL allows various levels of abstraction: from behavioral description (i.e. highest level of abstraction: the circuit's logic response is implemented) to gate level (i.e. the closest to hardware level: implements the functionality of the single logic gates). Moreover VHDL allows timing control, concurrent as well as sequential programming, and has library support. Every VHDL design consists of at least one entity/architecture pair, where the entity represents the interface of the circuit/component and the architecture describes the functionality and timing of the circuit/component. It is usually specified in terms of processes: the instructions within each process are executed serially, the processes are executed in parallel. More than one architecture can be implemented for the same component, but they are all mutually exclusive. In the design phase it is also essential to specify the links between each input/output line, defined in the FPGA design, with the real hardware pins. These and some other specifications concerning the hardware operations, e.g. operating voltages, clock frequency, signal types (i.e single ended or differential) are separated from the rest of the code and are stored in a dedicated file.
Once the design phase is completed, simulations allow to check if the circuit's behavior meets requirements and expectations. For this purpose the so called test bench is used. The test bench is written in VHDL as well as the circuit design and the two have very similar structure. The

test bench has basically three purposes: to generate the stimulus for the simulation, to apply this stimulus to the entity under test and to collect output responses, in terms of wave signals.
Examples of VHDL code will be shown in the next chapters.

Logic synthesis

The logic synthesis phase transforms an HDL design into a set of boolean gates and flip-flops. The synthesis tools transform the circuit design into a hierarchical boolean network, i.e. boolean logic gates, flip-flops and wiring connections among these elements.

Technology mapping

The technology mapping consists in the transformation of the boolean network, resulting from the synthesis process, into a functional equivalent k-LUT network that can be implemented in the FPGA. The objective of a technology mapping algorithm is to generate, among many possible solutions, an optimized one according to certain criteria (e.g. timing optimization, area minimization and power minimization).

Place & Route

Placement algorithms determine which logic block within an FPGA should implement the corresponding logic block required by the circuit. The optimization goals consist in placing connected logic blocks close together to minimize the required wiring, and sometimes to place blocks to balance the wiring density across the FPGA or to maximize circuit speed. Routing consists in assigning nets to routing resources such that none of these resources is shared by more than one net.

Timing analysis

Timing analysis has the purposes to determine the speed of circuits which have been completely placed and routed and to verify that performance specifications are met.

Bitstream generation

Once a netlist is placed and routed on an FPGA, the bitstream information is generated using the information coming from the technology mapping and the placement phase. The bitstream is then programmed on the FPGA using a bitstream loader. The configuration of the state of the memory bits in the FPGA is performed at this stage and it determines the implemented logical function.

Chapter 4

FPGA-based pulse generator

4.1 Hardware

For the prototyping phase of the flexible pulse generator it is decided to use an FPGA with average performances: LATTICE MachXO2 FPGA LCMXO2-7000HE-4TG144C from Lattice Semiconductor [21]. This FPGA is integrated in a 3" x 3" board, called MachX02™ Breakout Board (see Figure 4.1), which features the following components:

- FTDI chip [22] and USB mini-B connector for power and programming
- eight LEDs
- 60-hole prototype area
- four 2 x 20 expansion header landings for general I/O, JTAG, and external power
- 3.3 V and 1.2 V supply rails
- on-chip oscillator up to 133 MHz

This FPGA offers embedded flash technology for instant-on, non-volatile operation in a single chip. Numerous system functions are included, such as two PLLs and 256 kbits of embedded RAM plus hardened implementations of I2C, SPI, counter, and user flash memory. Flexible, high performance I/Os support numerous single-ended and differential

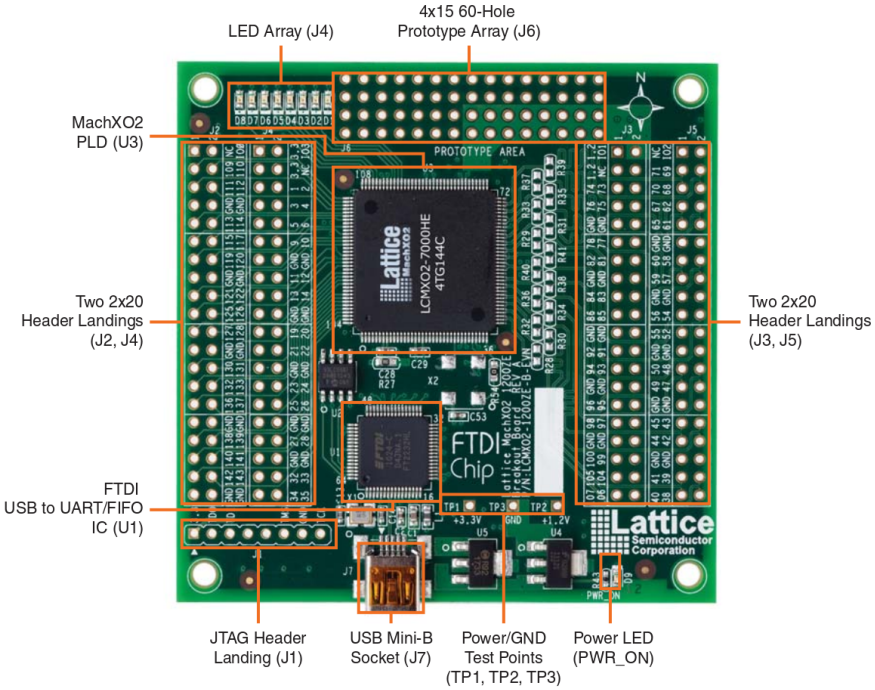

Figure 4.1: MachXO2 Breakout Board: top side [21].

standards including LVDS, and also source synchronous interfaces to DDR/DDR2/LPDDR DRAM memory. The 144-pin TQFP package provides up to 114 user I/Os in a 20 mm x 20 mm form factor [23]. The design software is provided by the selling company and it is called Lattice Diamond® [24].

4.2 The pulse generator: basic version

A pulse generator is basically a system or a device able to generate square waves at regular intervals synchronously with a clock signal, which has its own frequency. The basic elements that define the pulse are its period and its pulse width. The period is defined as the time between two rising edges of the signal (i.e the inverse of the frequency) and the pulse width is the time the signal is set to high logic level. These two parameters are specified in terms of clock cycles, which can be thought of as a metronome.

4.2.1 VHDL implementation

The function block diagram for the basic pulse generator is shown in Figure 4.2 and the entity declaration in Listing 4.1.

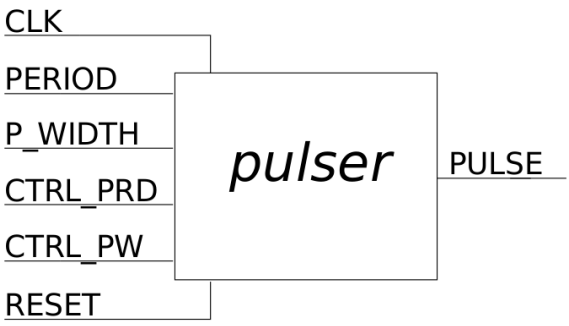

Figure 4.2: Function block diagram for the basic pulse generator.

```
entity pulser is

   port(
      CLK            : in std_logic;
      RESET          : in std_logic;
      PERIOD         : in std_logic_vector(31 downto 0);
      PULSE_WIDTH    : in std_logic_vector(31 downto 0);
      CTRL_PERIOD    : in std_logic;
      CTRL_PW        : in std_logic;
      PULSE          : out std_logic_vector(3 downto 0)
    );

end entity;
```

Listing 4.1: *pulser* entity declaration.

It features six inputs and one output. The inputs are respectively: the clock signal coming from the FPGA internal oscillator, an external reset signal (both single bit signals), the already introduced pulse width and period (32 bits signals) which can both be given by editing the code or via command line by using a slow control protocol and two single bit flags that switch value when either the period or the pulse width are changed.

The output is a single ended signal of four bits. The implementation of such a basic pulser is quite simple and can be performed defining a single entity with its own architecture. In Listing 4.2 is the main part of the architecture that shows how the pulse is generated.

```
if rising_edge(CLK) then
  if timer = unsigned(PULSE_WIDTH) then
    PULSE <= x"0" after 1 ns;
  elsif timer = x"00000000" then
    PULSE <= x"f" after 1 ns;
  end if;
end if;
```

Listing 4.2: Basic pulser architecture.

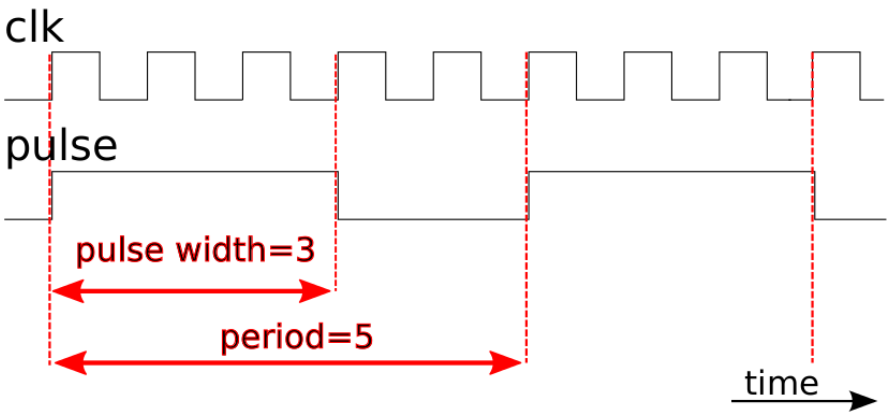

Figure 4.3: Signal representation of the clock signal and the pulse generated synchronously with its rising edge.

The first line is a condition on the rising edge of the clock, i.e. the next instructions are executed only if the rising edge of the clock occurs. This is the basic functionality of a flip-flop. *timer* is a counter for the clock cycles. When the number of clock cycles is equal to the selected pulse width then the signal goes to low logic level, vice versa when the number of clock cycles is zero, i.e. the system is in a reset condition, the pulse goes to high logic level. All the numbers are given in hexadecimal format. The syntax *after 1 ns* is ignored in the synthesis phase; it helps the

visualization of the signals in the simulation phase though. The result of such implementation is shown in Figure 4.3. The pulse is generated synchronously with the rising edge of the clock signal. In the present example the pulse width is set to 3 and the period is set to 5, meaning respectively 3 and 5 clock cycles.

4.3 A faster pulse generator

The implementation described in the previous section has a major drawback. As already mentioned, all the logic behind the generation of the pulses is ruled by the clock frequency. The FPGA internal oscillator can perform at 133 MHz maximum frequency (see 4.1). In terms of time, this translates into a period of 7.5 ns, which is far too large for the intended purpose of using these digital signals to drive LEDs to perform tests on the ECAL modules. Therefore, given the available hardware, the design has to be modified in order to achieve short pulses. The idea is to use the DDR output interfaces of the FPGA instead of the standard output. These special outputs allow to transfer the input data both on the rising and on the falling edge of the clock signal, i.e at double the rate with respect to the clock frequency. By doing so it is possible to generate the required short pulses.

4.3.1 VHDL implementation

The function block diagram for the new version of the pulse generator is shown in Figure 4.4. One more entity has to be defined: the DDR register (see Listing 4.3).

pulser entity

The declaration of the *pulser* entity is not changed with respect to the former version (i.e. it has the same inputs and outputs), but its architecture is modified in order to match with the newly insterted DDR entity (see Listing 4.4). The architecture is described in terms of a Finite State Machine (FSM). A FSM is conceived as an abstract machine that can be in one of a finite number of states, one state at the time (current state).

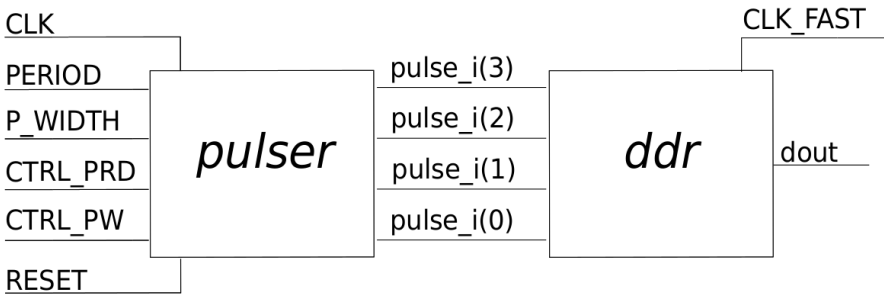

Figure 4.4: Function block diagram for the fast version of the pulse generator.

```
entity out5_ddr is
   port(
      clk_fast : in  std_logic;
      clk_slow : out std_logic;
      tristate : in  std_logic_vector(4 downto 0);
      data     : in  std_logic_vector(3 downto 0);
      dout     : out std_logic_vector(4 downto 0)
   );
end out5_ddr;
```

Listing 4.3: *out5_ddr* entity declaration.

It can change from one state to another when initiated by a triggering event or condition (transition). Thus, a FSM is defined by a list of its states, and the triggering condition for each transition. In the specific case the state diagram of the FSM is shown in Figure 4.5. The whole process starts only when the rising edge of the clock occurs and the system is not in a reset state. There are three possible states: *idle*, *generate_pulse* and *finish*. When the FSM is in the *idle* state, if the *timer* signal is zero then the output *PULSE* is set to the string "0000", i.e. basically no pulse signal at the output. Subsequently the FSM moves to the *generate_pulse* state and the pulse width given as an input is assigned to an internal signal (*pulse_width_i*), which can be manipulated in the next steps. If the *timer* signal is not zero then no changes occur and the FSM stays in the *idle* state. In the *generate_pulse* state a simple look-up table is implemented. If the pulse width is smaller or equal than four then:

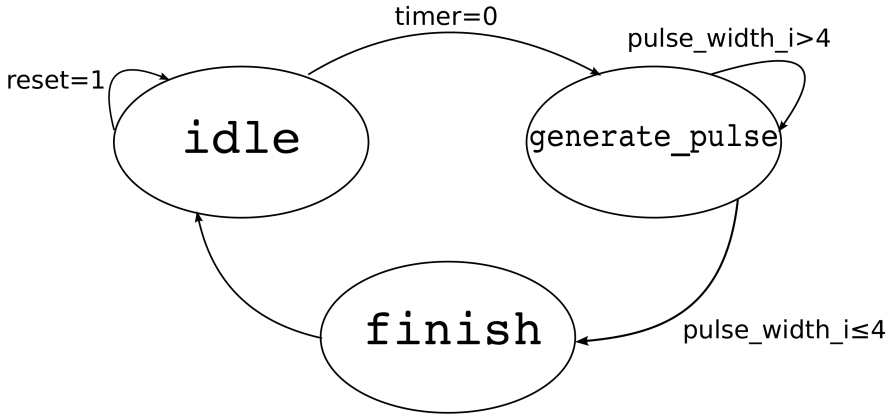

Figure 4.5: Diagram of the Finite State Machine used to implement the architecture of the *pulser*.

- pulse width = 1 corresponds to the string "1000"
- pulse width = 2 corresponds to the string "1100"
- pulse width = 3 corresponds to the string "1110"
- pulse width = 4 corresponds to the string "1111"

Each of these assignments occur within one clock cycle. If the pulse width is bigger than four then one more clock cycle is used to make the correct assignment. That is to say, the FSM will stay in the same state for the next clock cycle and it will check and compute the string that corresponds to the pulse width, given as input, minus 4 by using again the same look-up table. No transition occurs until the *pulse_width_i* is smaller or equal than four. When the assignments are completed then the FSM switches to the *finish* state and the process is concluded.

```
PROC_PULSE_MANAGER : process(CLK)
 begin
  if RESET = '1' then
    state <= idle;
  elsif rising_edge(CLK) then
    case state is
      when idle =>
        if timer = x"00000000" then
          PULSE <= "0000";
          state <= generate_pulse;
          pulse_width_i <= unsigned(PULSE_WIDTH);
        else
          state <= idle;
        end if;
      when generate_pulse =>
        if pulse_width_i = x"00000002" then
          PULSE <= "1100" after 1 ns;
        elsif pulse_width_i = x"00000003" then
          PULSE <= "1110" after 1 ns;
        elsif pulse_width_i >= x"00000004" then
          PULSE <= "1111" after 1 ns;
        else
          PULSE <= "1000";
        end if;
          pulse_width_i <= pulse_width_i-4;
        if pulse_width_i <= 4 then
          state <= finish;
        else
          state <= generate_pulse;
        end if;
      when finish =>
        state <= idle;
    end case;
  end if;
 end process;
```

Listing 4.4: Fast pulse generator architecture.

out5_ddr entity

The outputs of the first block, *PULSE_i*, are connected to the input of the second block (*data*). Each of these input bits is trasmitted to the output synchronously with the edges of the clock signal, both rising and falling, as characteristic of the DDR registers. This gives at the ultimate output the serialized version of the *data* inputs. The output actually consists of five lines and the user can decide to enable one or more of these lines by setting the value of the *tristate* signal, e.g. the string "11110" would enable only the LSB of the output *dout* (inverse logic). At the moment all the five lines carry the same signal. As shown in the function block diagram (Figure 4.4), the two blocks are governed by two different clock domains, namely the *clk_slow* and the *clk_fast*. The *clk_fast* is coming from the FPGA internal oscillator. The *clk_slow* is generated inside the *out5_ddr* block by a clock divider, which is the reason why it is defined as an output signal in the entity declaration, and thus available to be sent to the *pulser* block.

4.3.2 Simulations

The design is simulated by using the software ModelSim® by Mentor Graphics [25]. Two examples of the simulation are shown in Figure 4.6 and Figure 4.7. On the top are the two clock signals, one with frequency double than the other. Right below are the input control flags and the reset signal, all active high, showing that the inputs have changed. Following are the output of the *pulser* and the ultimate output. Pulse width and period are given in terms of the fast clock signal. In the first example (Figure 4.6) the selected pulse width is two and it actually corresponds to the output sequence "1100", *pulse_i(0)* and *pulse_i(1)* are both set to high logic level, whilst *pulse_i(2)* and *pulse_i(3)* are set to low logic level. The *dout* signal shows how each of the four bits coming from the *pulser* is transmitted when the edges of the fast clock signal occur, both rising and falling. In the second example (Figure 4.7) the pulse width is set to five. It corresponds to the output sequence "1111", computed in one slow clock cycle, plus the sequence "1000" computed in the next clock

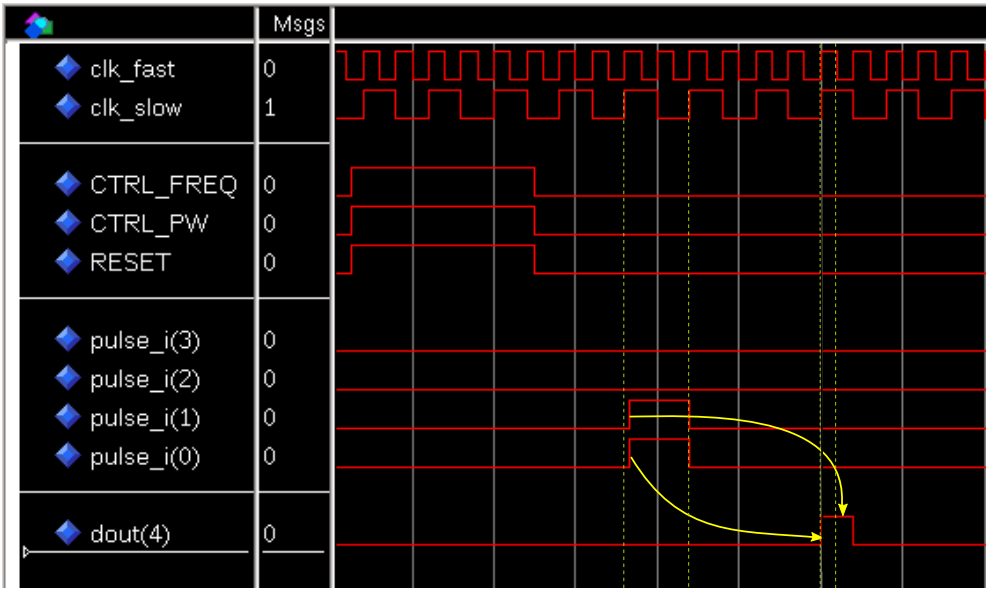

Figure 4.6: Simulation of the fast pulse generator: pulse width is set to two.

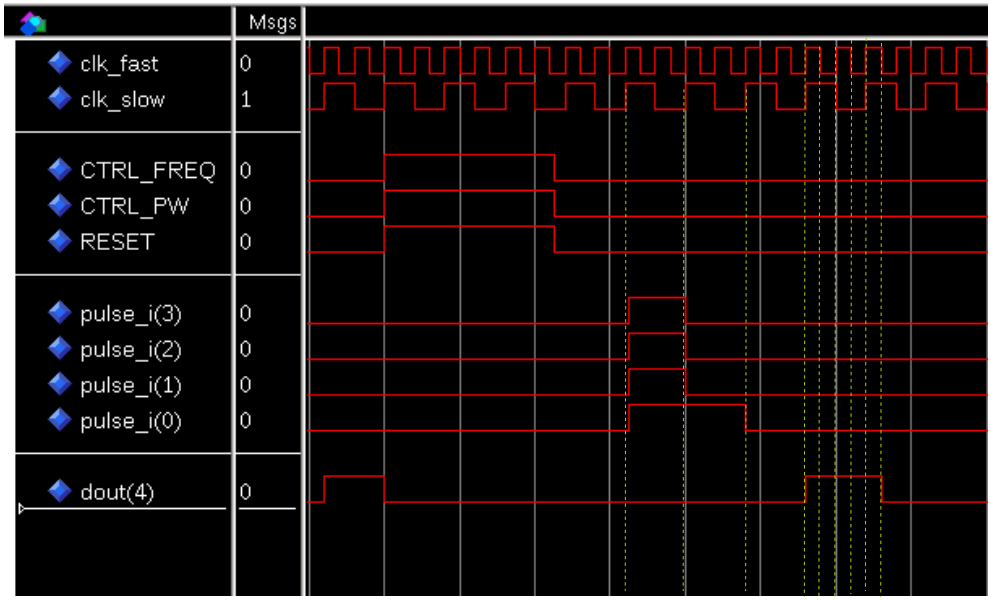

Figure 4.7: Simulation of the fast pulse generator: pulse width is set to five.

cycle. The high level bits are thus transmitted to the output within five consecutive edges of the fast clock signal.

This implementation allows to produce shorter pulses with respect to the former design which does not make use of the DDR outputs. In fact, in the present case the minimum pulse width is half the period of the fast clock. Assuming that the fast clock is coming from the FPGA internal oscillator running at its maximum frequency of 133 MHz, the slow clock generated from the clock divider has 66.5 MHz frequency, the *dout* signal transmits at 266 Mbit/s. Thus, the minimum pulse width is around 4 ns. Shorter pulses can be achieved by using an external oscillator to generate the fast clock.
Thus the fast pulse generator meets the requirements related to its usage as LED driver for monitoring and calibration of the ECAL modules. Moreover, although some more features should be included, the design is also suitable for testing of the TDCs implemented in the digitization board TRB3 (see Section 2.3.2). For they accept digital inputs, it is possible to connect the pulse generator directly to the input, instead of going through the whole read-out chain, to check their behavior.

Chapter 5

Hybrid pulse generator

The FPGA-based pulse generator, as widely discussed in Chapter 4, allows for testing of two of the main blocks of the read-out chain, namely the calorimeter modules and the TDCs implemented on the TRB3. There is though another element in the read-out chain, namely the front-end board PADIWA AMPS, that could still be tested by reusing the previous results and adding some more components. This board does not accept digital inputs, so the FPGA-based pulse generator cannot be connected directly to it. However, still following the COME & KISS concept (see 2.3), a system for testing of the PADIWA AMPS board can be built.

5.1 Basic idea and requirements

The basic idea behind the design of the hybrid pulse generator to perform tests of the PADIWA AMPS board is to send the digital signal coming from the FPGA to a rather simple analog circuit. This simple circuit shapes it and makes it similar to the signals coming from the ECAL PMTs known from previous tests with LEDs, cosmics rays and photons [26]. Typical shapes of these signals are shown in Figure 5.1. The following parameters are assumed as indication for the pulse that has to be generated [1]:

[1] for definition of rise time and falling time see 5.2.2

- rising time $\sim$ 3 ns
- falling time $\sim$ 50 ns
- frequency $\sim$ 10 kHz
- amplitude: 500 mV - 1.5 V

5.2 First version

5.2.1 Design

The square wave coming from the FPGA is sent to an amplification and inversion stage. This stage consists of a single bipolar transistor. A resistor is placed between the power supply and the base to realize a fixed (or base) biasing [28], as shown in Figure 5.2. In fact, by applying the Kirchhoff's second law to this circuit, one obtain $V_{cc} = I_b \cdot R_b + V_{be}$ and thus $I_b = (V_{cc} - V_{be})/R_b$. For a given transistor, V_{be} does not vary significantly during use. As V_{cc} is of a given value, on selection of R_b, the

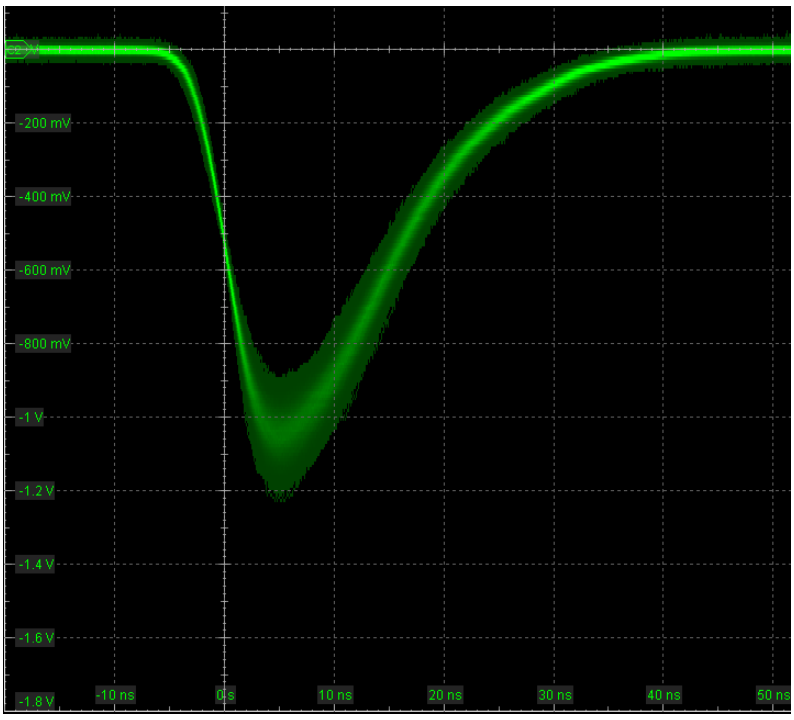

Figure 5.1: Signal from ECAL tests with LED [27].

base current I_b is fixed. Therefore this type is called fixed bias and allows to set the operating point of the circuit anywhere in the active region by merely changing the base resistor. An inductor is placed between the power supply and the collector of the transistor to preserve the integrity of the signal, preventing the high frequencies to flow through this path. The rising time of the output signal depends on the pulse width of the one coming from the FPGA. However, to be sent as input to the base of the transistor, this digital signal needs some shaping. For this purpose a resistor and a capacitor in series are placed in the input line. The resistor size defines the amplitude of the output signal, the capacitor cuts the DC component of the incoming signal. At this point only the amplitude and the rising edge are thus adjustable, by varying respectively the resistor size and the pulse width of the digital signal. Shaping of the falling edge is also possible though, by mean of a capacitor placed between the collector and ground. This capacitor basically integrates the signal, so the bigger the capacitor, the longer the tail. Moreover, since a DC offset is still present at the collector of the transistor, another capacitor in parallel with the previous one is added to restore the baseline to zero. To avoid reflection in the cable a terminating resistor is used. As shown in Figure 5.3, the schematic of the analog circuit is rather simple and includes only few components. The 12 Ω resistor in series with the inductance simply emulates its internal resistance. The 2 Ω resistor placed from the emitter to ground has the only purpose of making the circuit response a bit faster.

5.2.2 Simulation

For the simulations of the circuit, the software tool LTspice is used. It allows to simulate the circuit providing different kinds of analysis tools such as: DC analysis to choose the operating point, AC analysis showing the frequency response, transient analysis showing the behavior of a voltage or current as a function of time. Moreover, by using the *.MEAS* and the *.STEP* command respectively, it is possible to perform measurements on the result of the analysis, such as time, frequency, maximum and minimum value of an observable, and to instantiate one or more component

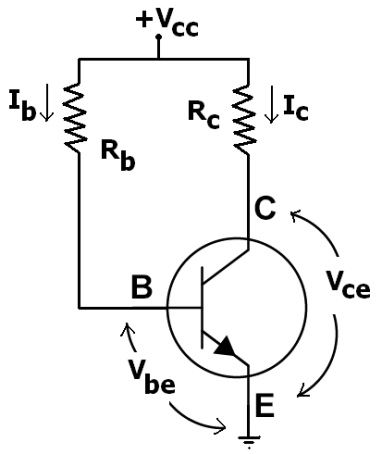

Figure 5.2: Bipolar transistor with fixed bias [29].

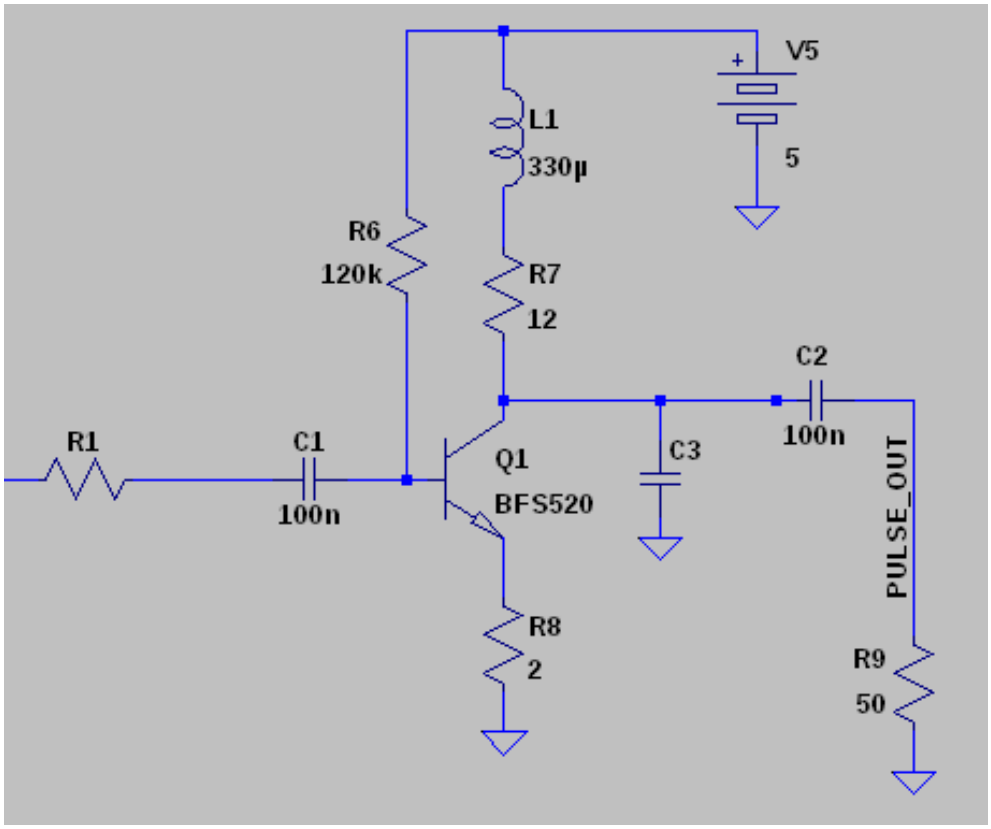

Figure 5.3: Schematic of the analog circuit to be connected to the outputs of the FPGA to perform testing of the PADIWA AMPS board.

as parameters, in order to define a list of different values to be assigned in successive iterations. Example of the usage of these commands will be shown in this section.

The FPGA output signal is emulated by using a voltage source generating square waves with high level equal to 3.3 V. Transient simulations are performed with different values for the components. For each run, the time at which the signal reaches the maximum amplitude and its value, the rising time and the pulse length are calculated and stored in a file. The rising time is defined as the time required for the signal to rise from 10% to 90% of its maximum value. The pulse length is given in terms of time over threshold, i.e. the difference in time corresponding to the two crossing points of a given threshold. In the present case the threshold is set to 10% of the signal maximum. The instructions to perform the measurements are shown in Listing 5.1. Figure 5.4 shows the result from

```
.MEAS TRAN V_peak MIN V(PULSE_OUT)
.MEAS TRAN t_peak WHEN V(PULSE_OUT)=V_peak
.MEAS TRAN V1 param (V_peak*0.9)
.MEAS TRAN V2 param (V_peak*0.1)
.MEAS TRAN t1 V(PULSE_OUT) WHEN V(PULSE_OUT)=V1
.MEAS TRAN t2 V(PULSE_OUT) WHEN V(PULSE_OUT)=V2
.MEAS TRAN t_rise param (t1-t2)
.MEAS TRAN t3 V(PULSE_OUT) WHEN V(PULSE_OUT)=V2 cross 2
.MEAS TRAN tot param (t3-t2)
```

Listing 5.1: LTspice instruction.

a simulation performed by choosing a fixed value for C3 and different values for R1. Each curve corresponds to a given R1. The rising and falling time are roughly the same for all the curves, but the amplitude is variable between 740 mV and 4.4 V, depending on the resistor size, as expected. Obviously, the smaller the resistor, the bigger the amplitude. Choosing a fixed value for R1 and different values for C3 (see Figure 5.5), it is possible to see how the size of the capacitor actually shapes the falling edge of the signal. As one can expect, the amplitude is partially

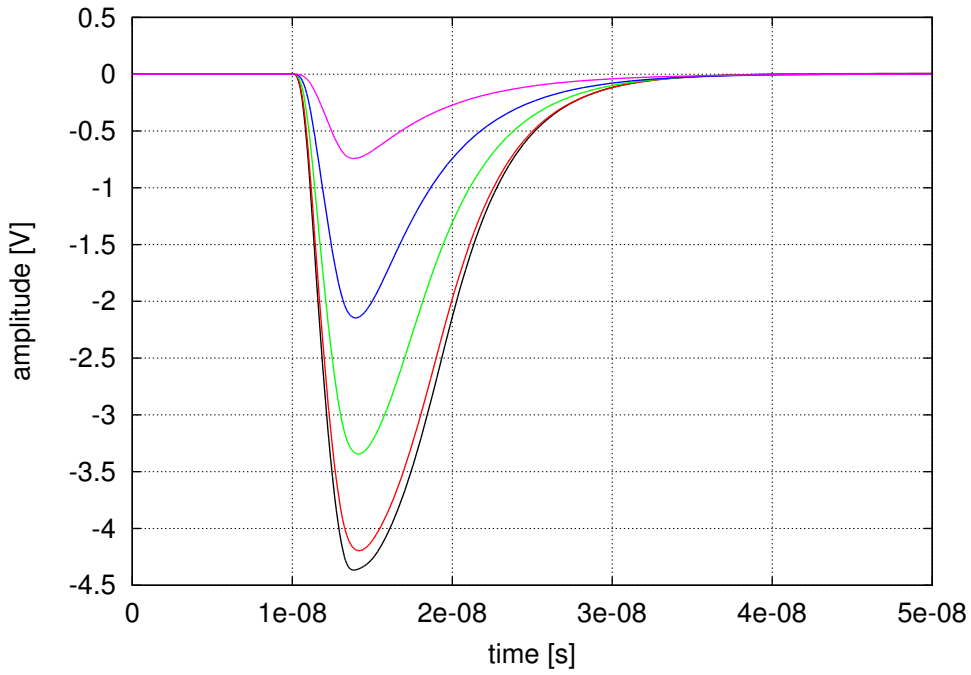

Figure 5.4: Simulation of the analog circuit with R1 = 0.39 (black), 0.47 (red), 0.82 (green), 1.8 (blue), 6.8 kΩ (violet), C3 = 56 pF and pulse width = 1.25 ns.

influenced by the size of this capacitor, since it is performing an integration of the incoming signal. As a matter of fact, a big capacitor does not allow to reach the maximum amplitude for a fixed resistor size. In both these examples the digital pulse width is set to 1.25 ns. Figure 5.6 shows the influence of the pulse width of the digital pulse on the rising time: the rise time increases linearly with the increasing of the digital pulse width.

At the simulation level, the designed circuit meets the requirements mentioned above. The shape of the signals is very similar to the sample, the rise time can be easily set to values even smaller than the reference one, which is around 3 ns, the amplitude can be selected in the desired range (500 mV - 1.5 V) and further, as well as the falling time. Nevertheless, this pulse generator has a main drawback: the lack of flexibility. As the output pulse shape is fixed for a given combination of resistor, capacitor and pulse width, if the user wants to change the parameters of the pulse the only possible solution is to replace the discrete components.

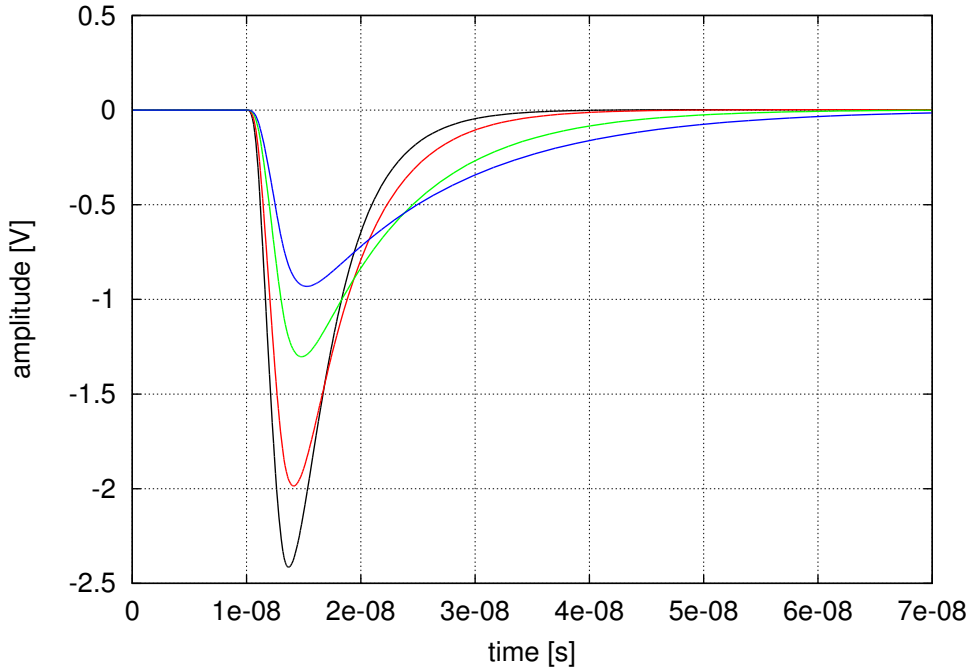

Figure 5.5: Simulation of the analog circuit with R1 = 1.8 kΩ, C3 = 39 (black), 68 (red), 150 (green), 245 pF (blue) and pulse width = 1.25 ns.

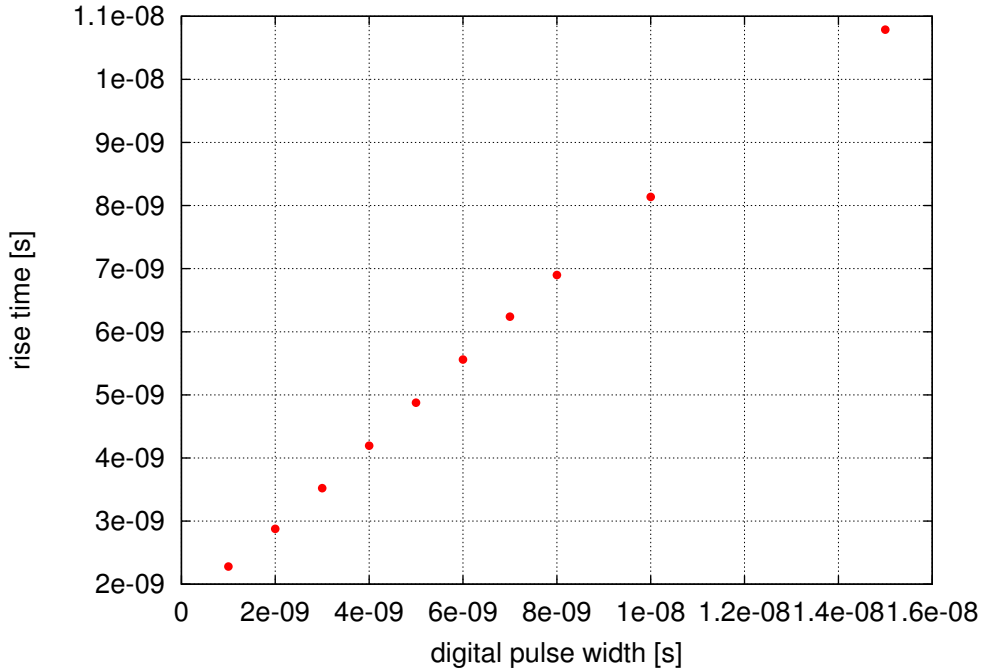

Figure 5.6: Rise time as a function of the digital pulse width for R1 = 1.8 kΩ and C3 = 150 pF.

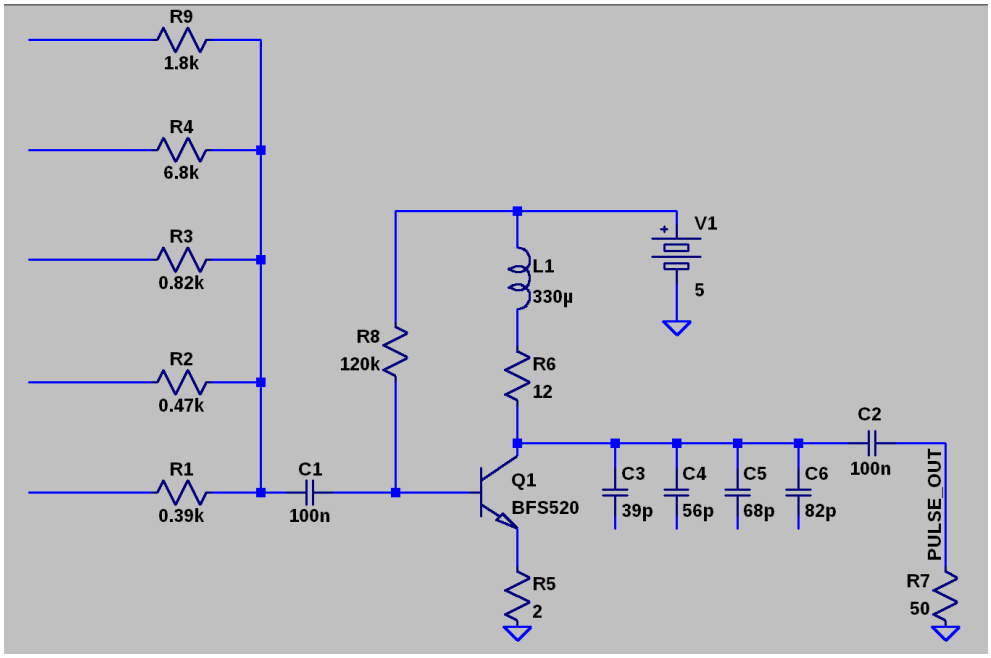

Figure 5.7: Schematic of a more flexible analog circuit to be connected to the outputs of the FPGA to perform testing of the PADIWA AMPS board.

5.3 A more flexible version

To overcome this issue a simple solution is implemented. The principle stays the same, but instead of using a single resistor and a single capacitor, several of them are added in parallel to the previous R1 and C3 (see the schematic in Figure 5.7). Each of them is connected to an output pin of the FPGA, by mean of which it can be enabled or disabled remotely. Disabled resistors are connected to ground, disabled capacitors are set to high impedance. If more than one resistor is enabled, the same signal is sent from the FPGA to the corresponding input lines and an analog sum is performed at the node that precedes the decoupling capacitor C1. The equivalent resistance has to be considered in order to obtain the desired amplitude. The capacitors are enabled when connected to ground, otherwise they represent a high impedance path that does not influence the equivalent capacitance. The values chosen for the resistors and capacitors are respectively: 0.39 kΩ, 0.47 kΩ, 0.82 kΩ, 1.8 kΩ, 6.8 kΩ and 39 pF, 56 pF, 68 pF, 82 pF. The smallest input resistor is chosen

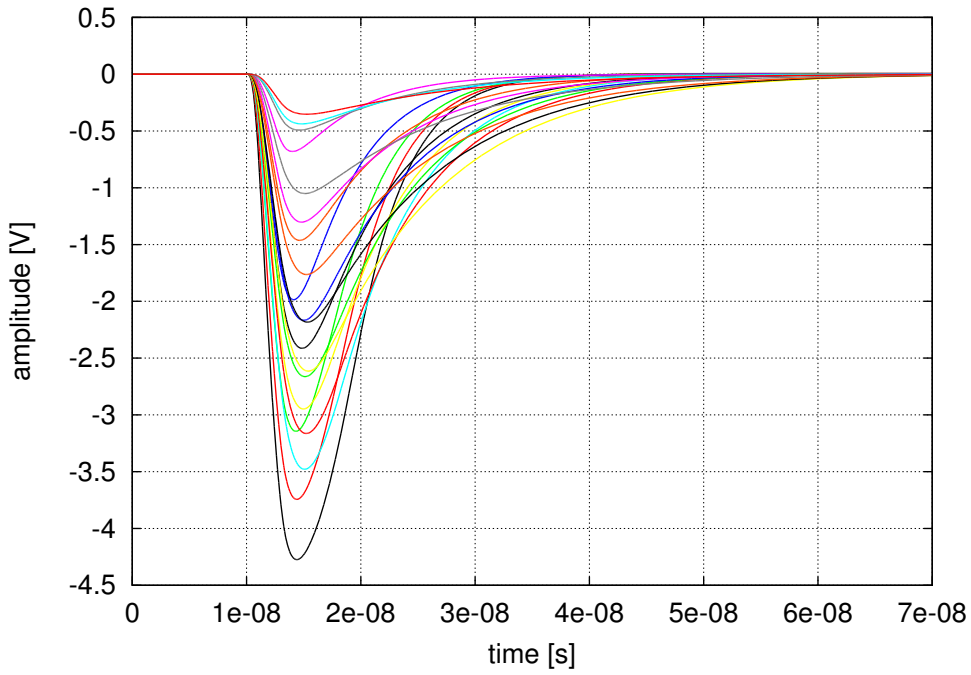

Figure 5.8: Simulation of the flexible analog circuit with $R_{eq} = 0.39$, 0.56, 0.82, 1.8, 6.8 kΩ, $C_{eq} = 68$, 124, 150, 207 pF and pulse width = 1.25 ns.

to be 0.39 kΩ, for smaller values produce a large input signal that causes the saturation of the transistor. The biggest input resistor is chosen to be 6.8 kΩ, for bigger values lead to signals with an amplitude smaller than 400 mV, not interesting for the intended purpose. The capacitors size are chosen such that the output pulse shape is similar to the sample already shown in Figure 5.1. Results of the simulations can be found in Figure 5.8. Figure 5.9 shows the rise time as a function of the time over threshold for all the possible combinations with the chosen components. Each data point corresponds to a different value of the equivalent resistance and equivalent capacitance. Data point belonging to the same line correspond to the same equivalent resistance but different capacitance. The dependence is linear and the slope decreases with the increasing of the resistor size, i.e. the rise time for signals with small amplitude exhibits weaker dependence on the time over threshold than those with the large amplitudes.

This latter implementation allows thus to obtain different shapes of the analog pulse, by changing only the enabled/disabled components re-

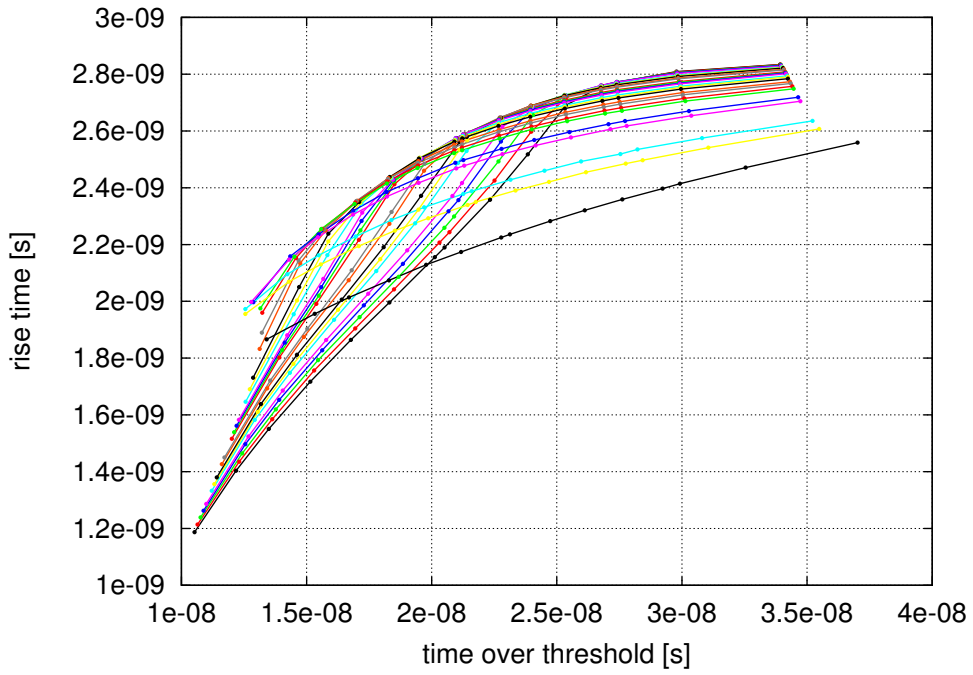

Figure 5.9: Rise time as a function of the time over threshold for all the possible combinations with the chosen discrete components.

motely on the FPGA level, without having to replace any component hardware-wise. The approach goes in the direction of the desired flexibility, that will allow systematic tests of the PADIWA AMPS board.

5.4 Extra features

5.4.1 Symmetric and attenuated pulses

The signals coming from the hybrid pulse generator emulate rather well the ones produced by particles into the ECAL modules, exhibiting a fast rising edge and a slow falling edge. Output signals from other detectors currently present in the HADES set-up, can be more symmetric with very fast rising as well as falling edge, e.g. diamond detectors (see Figure 5.10). Therefore, it is worth to consider some extra features for the hybrid pulse generator, to make it suitable for testing different kinds of detectors. Rather symmetric pulses can be generated by simply adding a small resistor (smaller than or comparable to the 50 Ω termination resistor)

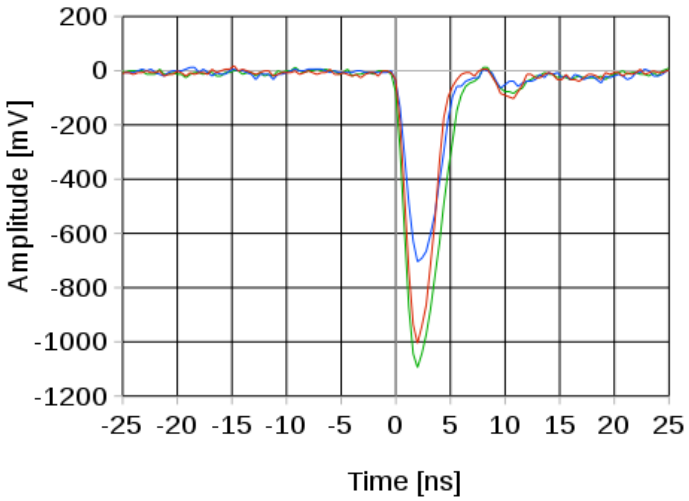

Figure 5.10: Signals from the HADES start diamond detector.

between the output line and ground. This resistor can be connected to an FPGA output pin and be enabled/disabled remotely according to the user needs. In this way, it is allowed to choose only a single value for the resistor. Modifying the response would be possible only by substituting the resistor with another one of a different size. However, the additional resistor modifies the load of the transistor and can then be used as an attenuator for the signal amplitude. There is an alternative way of generating symmetric pulses which does not involve the introduction of any additional hardware. Two outputs of the FPGA can be used to provide signals with opposite polarity, one delayed with respect to the other, as inputs of the analog part. Each of these, individually, would generate either a positive or a negative output pulse. An analog sum, performed by sending these two signals to two input resistors respectively and then to a common node preceding the decoupling capacitor, results in a pulse with shorter tail. The fast falling edge is due to the fact that the signal is forced to go back to the baseline by the delayed signal, which

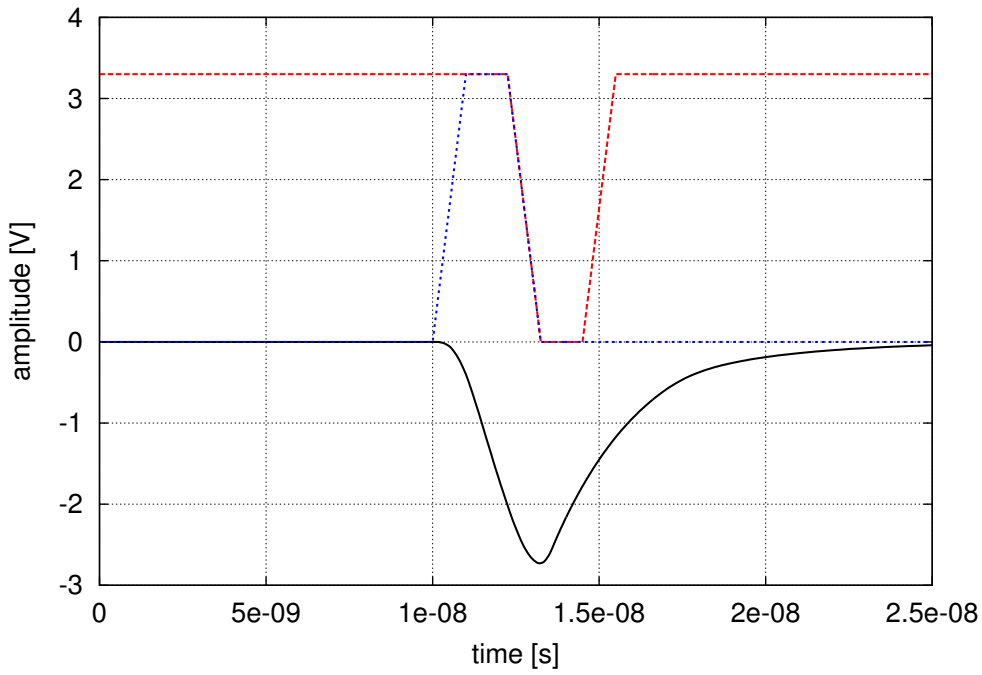

Figure 5.11: Digital input pulses with opposity polarity, one delayed with respect to the other; output pulse shows a shorter tail (red).

has opposite polarity with respect to the first one. The output shape can be modified by changing the values of the input resistors. Depending on the ratio between the two input resistors, the output can exhibit an overshoot. The shaping capacitors can be used to minimize it, if needed. Figure 5.11 shows the digital input signals and the output pulse for a run with the following components values: $R_{input1} = R_{input2} = 0.82$ kΩ and $C_{eq} = 56$ pF. Figure 5.12 shows the rise time as a function of the time over threshold for the more symmetric outputs. The rise time appears to have a weaker dependence on the time over threshold, with respect to the non symmetric pulses (cf. Figure 5.9). This is due to the fact that the falling edge, and then the time over threshold, is mostly determined by the digital signal with negative polarity, which forces the output pulse to go back to the baseline. Figure 5.13 is the same as Figure 5.9 but includes also the data points corresponding to the more symmetric pulses, showing the coverage in terms of pulse shapes for the specified uses.

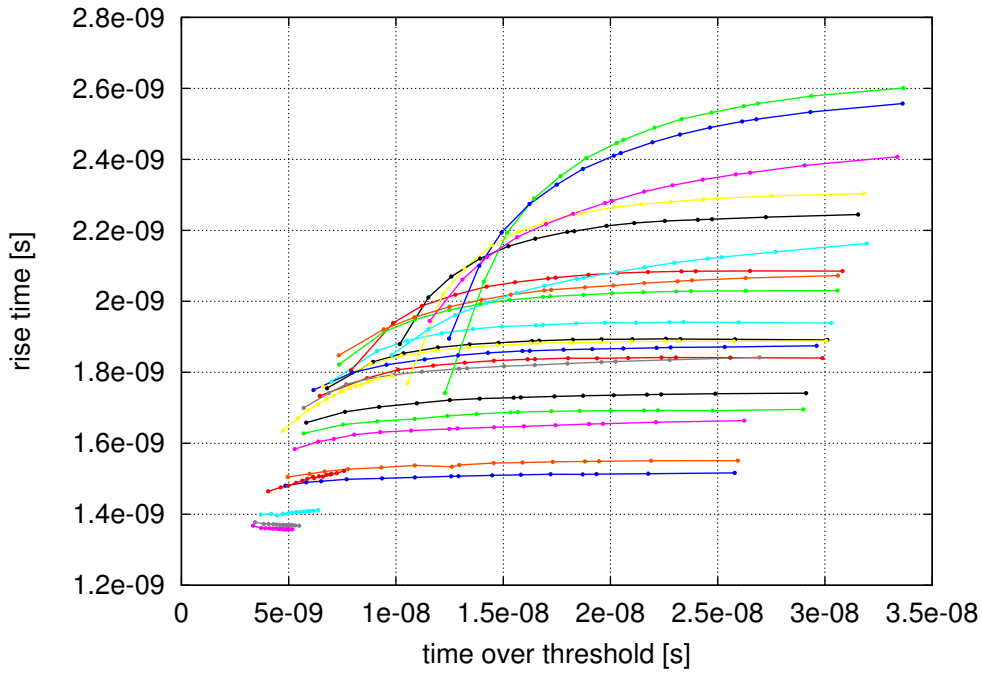

Figure 5.12: Rise time as a function of the time over threshold for all the possible combinations with the chosen discrete components for more symmetric pulses.

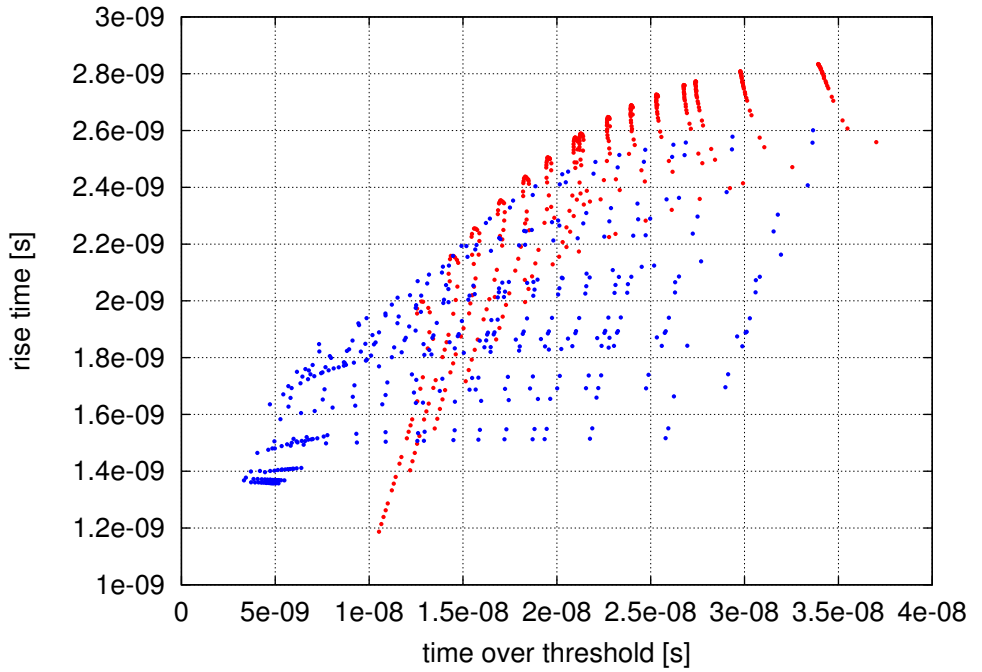

Figure 5.13: Rise time as a function of the time over threshold for all the possible combinations with the chosen discrete components: red dots correspond to the asymmetric pulses and blue dots correspond to the more symmetric pulses.

Chapter 6

Tests on the pulse generators

6.1 Tests on the hybrid pulser

In the previous chapters the design of the FPGA-based pulse generator and of the hybrid pulse generator were shown, together with their simulations. The behavior of the pulsers on the real hardware has to be tested in the laboratory. It was decided to test first the hybrid pulse generator to check the behavior of the two pulsers (digital and analog) at once, for the analog part needs to be driven by the digital pulse generator.
The data shown in this chapter have to be taken as the results of a first approach to the testing of the device. Therefore no quantitative measurements are presented here.

6.1.1 Qualitative measurements with MachXO2

Figure 6.1 shows the prototype board that has been commissioned and used in this testing phase. It implements the circuit shown in the schematic on Figure 5.7. Several housings for any additional components, e.g. input and pull down resistors and shaping capacitors are included. The discrete components have to be soldered by the user.

The MachXO2 Breakout Board is connected via its USB port to a PC for power supply and for slow control. Its output signals are sent to the input lines of the analog board. The power supply for the analog board is provided by GW INSTEK PSP-405 and it is set to 5 V. The two boards are both connected to a common ground, namely the ground pin provided by the MachXO2. The real circuit produce an output pulse

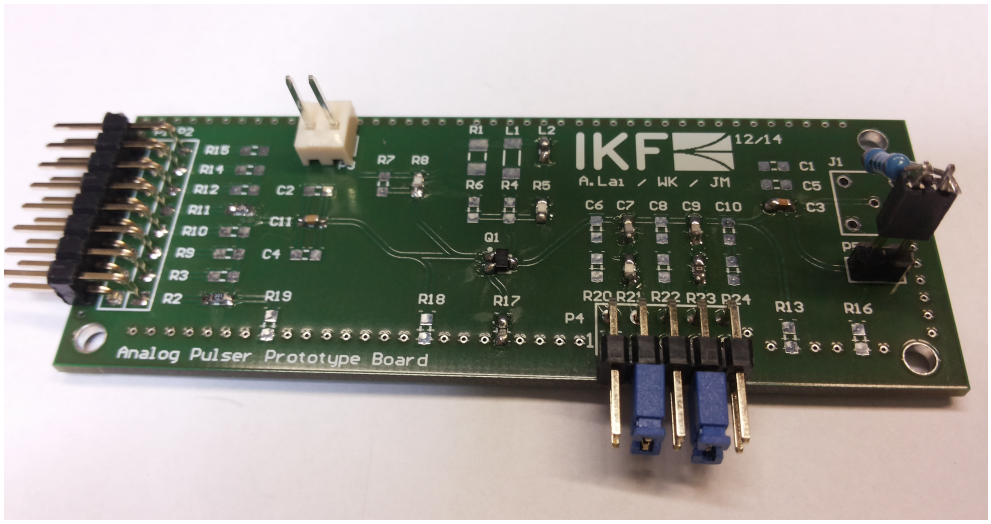

Figure 6.1: Prototype of the analog board for the hybrid pulse generator.

which is quite similar to the simulated one, though some oscillations and an overshoot are present. Oscillations might be caused by the inductance present in the circuit combined with some parasitic capacitance. It is known that the resonant effect of an LC circuit is relevant mostly for high frequencies. Therefore to remove this oscillation effect one can use a filter, for example a ferrite bead. A ferrite bead is a passive electric component that suppresses high frequency noise. Behaving as a resistor for such frequencies, dissipates the current in a ferrite ceramic in the form of heat. A ferrite bead (Murata BLM18PG471) is thus added in the circuit between the transistor collector and the power supply. Another plausible hypothesis is that some noise is coming from the power supply and/or from ground. Therefore all the cables are the shortest possible and another filter, built using again ferrite beads and some capacitors, is put in (see Figure 6.2). One more idea to reduce noise is to use the differential outputs of the FPGA instead of the single ended ones. LVDS is a differential signaling system, meaning that it transmits information as the difference between the voltages on a pair of wires. The two wire voltages are compared at the receiver. In a typical implementation, the transmitter injects a constant current of 3.5 mA into the wires. The current passes through a termination resistor of about 100 to 120 Ω, matched to the cable's characteristic impedance to reduce re-

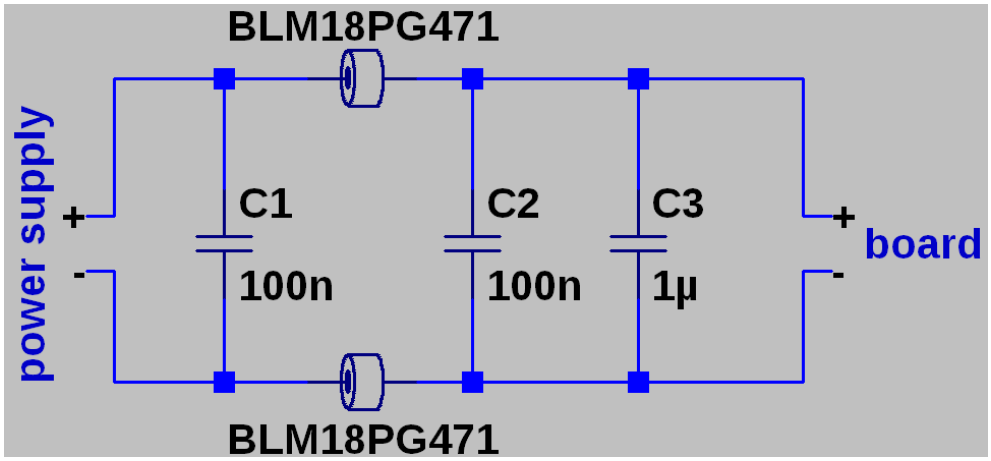

Figure 6.2: Filter for the power supply line.

flections, at the receiving end and then returns in the opposite direction via the other wire. From Ohm's law, the voltage difference across the resistor is therefore about 350 mV. The receiver senses the polarity of this voltage to determine the logic level. As long as there is tight electric and magnetic field coupling between the two wires, LVDS reduces the generation of electromagnetic noise. This noise reduction is due to the equal and opposite current flow in the two wires creating equal and opposite electromagnetic fields that tend to cancel each other. In addition, the tightly coupled transmission wires will reduce susceptibility to electromagnetic noise interference because the noise will equally affect each wire and appear as a common-mode noise. The LVDS receiver is unaffected by common mode noise because it senses the differential voltage. Since the analog board needs a single ended input signal, the LVDS output from the FPGA has to be converted into TTL. The converter by National Semiconductor, Mod.DS90LV012, [30] is placed as intermediate stage between the FPGA outputs and the analog board inputs. Having this device in the set-up needs some additional care. As explained in Section 5.3, the input resistors can be enabled and disabled remotely on the FPGA level. In principle a tristate signal can be used, allowing the FPGA output to be in a high impedance state in addition to the 0 and 1 logic levels. By doing so, when the FPGA output is set to high impedance, the LVDS to TTL converter is not powered. There might be

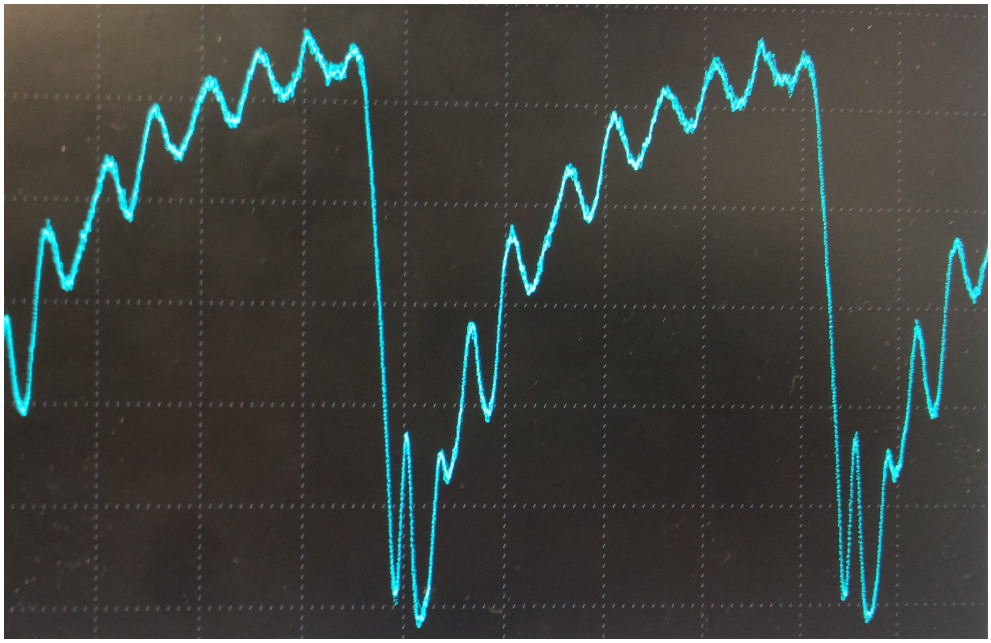

Figure 6.3: Screenshot from the oscilloscope shows the amplitude versus time of the hybrid pulser output signal (arbitrary units).

some flow of current from the output to the input of the converter that can thus power up the whole circuit, leading to undesired effects. This possible behaviour is actually proved by driving the output with a 3 V signal, resulting in uncontrollable oscillations. Thus the input resistors have to be driven with a non-tristate signal to avoid the high impedence state.
In Figure 6.3, a screenshot from the oscilloscope shows the shape of the signal after the introduction of the additional components. As one can see, despite the adopted measures to reduce noise, some oscillations are still present.

6.1.2 A different approach for the pulser using TRB3

A different approach for the implementation of the hybrid pulser is considered. Currently, an ongoing group project foresees the design of a new FPGA custom board smaller than the TRB3. This board will feature many I/O pins running at a speed up to 1 GHz (the MachXO2 board has only nine high speed output pins) and would be suitable for the

implementation of the full-featured pulser. For the moment, since this board is not yet ready, the digital design is implemented in a regular TRB3, even though this board is far too big for the intended purpose, which will be replaced afterwards, hopefully with not much effort. The analog circuit can be implemented in an Add-On to the TRB3, compatible with the future board. This way, any eventual noise related to the connection cables among the components would be removed, gaining in terms of quality of the signal.
The already tested design is implemented in one of the TRB3 peripheral FPGAs. No substantial changes are needed, except for a few additional lines of code to meet the timing: since this FPGA is bigger, the routing can affect the timing differently than in the smaller FPGA. Moreover, the slow control has to be modified in order to use the existing TRBnet communication protocol [31]. An on-board oscillator can work at frequencies up to 200 MHz. By mean of a PLL a 400 MHz frequency clock is generated, i.e. 800 Mbit at the DDR output. This value allows to produce signals with 1.25 ns minimum pulse width.

The set-up is shown in Figure 6.4. The TRB3 board is powered by a Voltcraft FSP 4805 power supply with 48 V. A 32 pin Add-On board to the TRB3 is used (top left on the board). The yellow square is the breadboard onto which the LVDS to TTL converter is soldered. It is connected to the TRB3 pins that provide 3.3 V power supply and ground connection. At the moment, only one output is provided, allowing to use only one input of the analog board at the time. The analog board is powered with 5 V using the GW INSTEK PSP-405, as previously. For simplicity, the shaping capacitors, if enabled, are connected to ground by mean of jumpers. In a next step they will be connected to the output pins of the FPGA and enabled/disabled remotely, as already explained in 5.3. The output, terminated with 50 Ω is then sent to an oscilloscope. Following are some qualitative results.

Using one of the TRB3 FPGA, instead of the MachX02, to generate the digital pulse results in a better quality of the output signals, concerning the noise. The digital part of the circuit is actually able to generate very short signals. To have a precise measure of the minimum achiev-

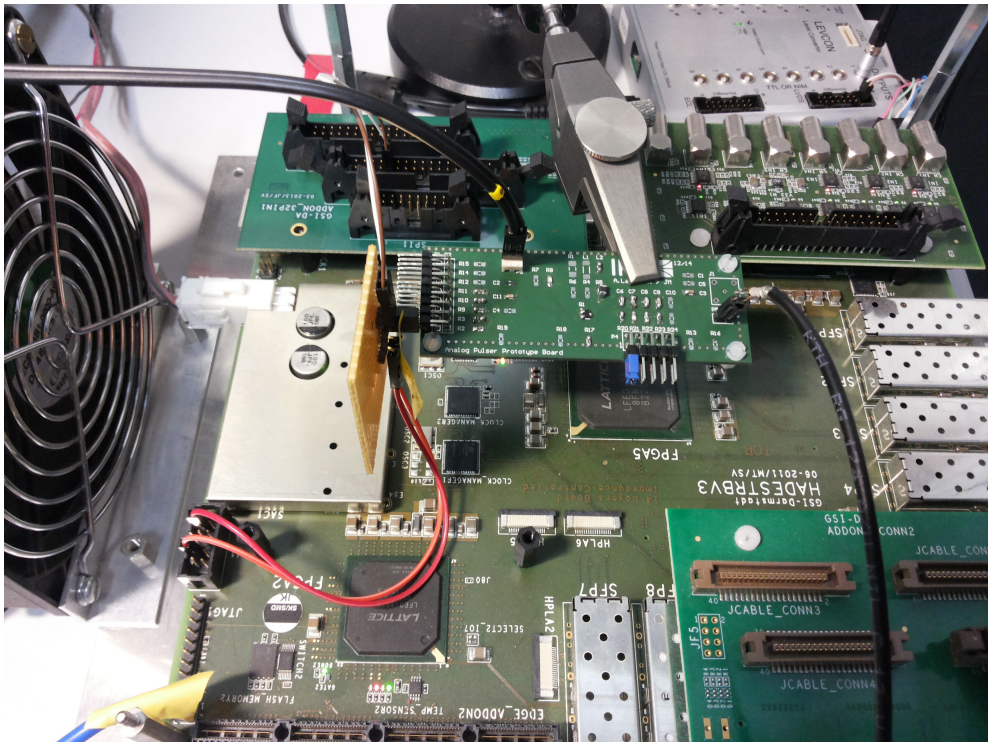

Figure 6.4: Set-up for the tests using the TRB3.

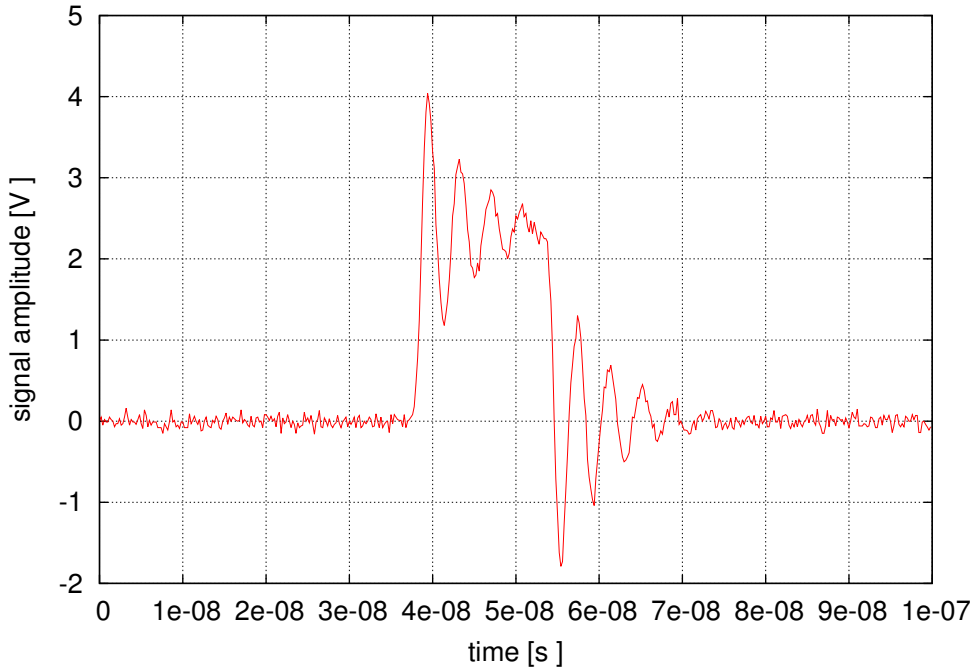

Figure 6.5: Input signal to the analog board; digital pulse width is set to 25 ns.

able pulse width, a more compact set-up is needed. As a matter of fact, the reflections introduced by the cables used to connect the components together make the measurement unreliable. As an example, the input of the analog board (i.e. the digital LVDS signal after the conversion into TTL) is shown in Figure 6.5 for a pulse width of 25 ns. Figure 6.6 and 6.7 show the output pulse produced by the circuit choosing the same value of the enabled resistor and two different values of the equivalent capacitance, respectively 39 pF and 189 pF. The pulse corresponding to a larger shaping capacitance exhibits a longer tail, while the rise time appears to be approximately the same in the two cases. The amplitude appears to be reduced from 2.5 V to 1.8 V, with the increasing of the capacitor size.

The behavior of the hybrid pulse generator is rather consistent with the simulations (cf. Figure 5.5), despite the fact that the achieved amplitudes are smaller than expected. This effect might be caused by a not exact reproduction of the behavior of the ferrite bead and/or the transistor in simulation. However, this does not represent an obstacle for the purpose of the pulse generator, which is meant to be used for generation of pulses with amplitude smaller than 2 V. Comparing Figure 6.6 with 6.8 one can see how the resistor size actually defines the amplitude, which is reduced by a factor ten going from a 0.39 kΩ resistor to a 6.8 kΩ resistor.

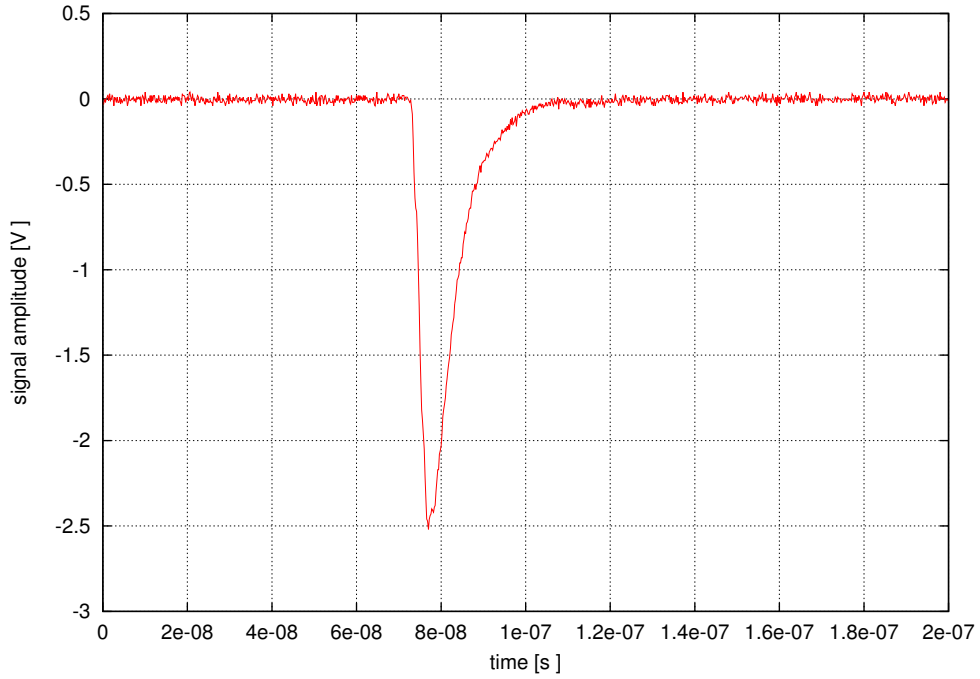

Figure 6.6: Output pulse produced by the real circuit when R = 0.39 kΩ and C = 39 pF; digital pulse width is set to 1.25 ns.

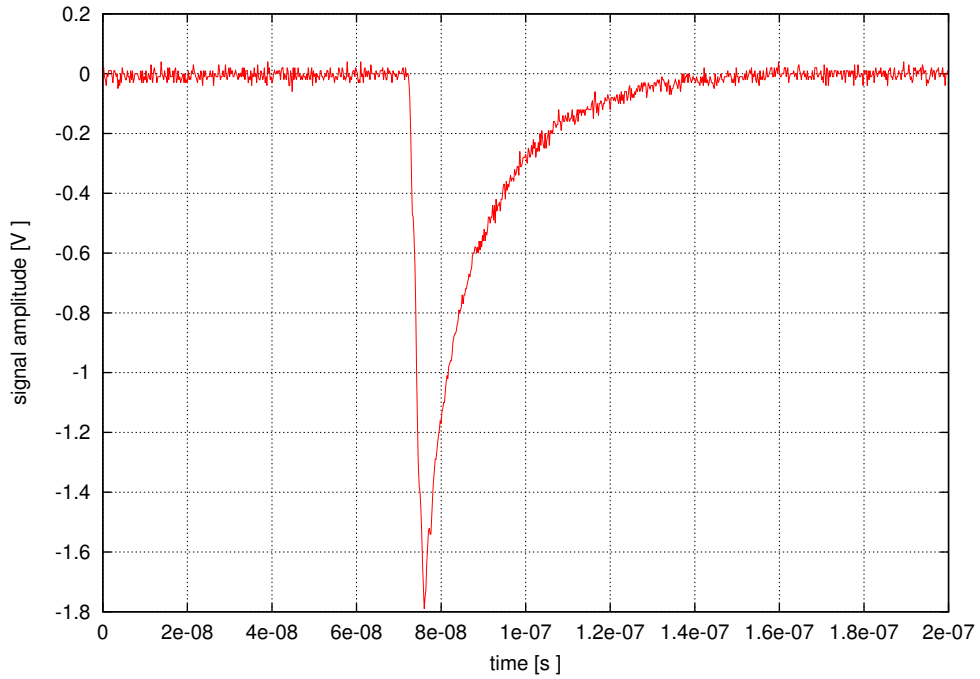

Figure 6.7: Output pulse produced by the real circuit when R = 0.39 kΩ and C = 189 pF; digital pulse width is set to 1.25 ns.

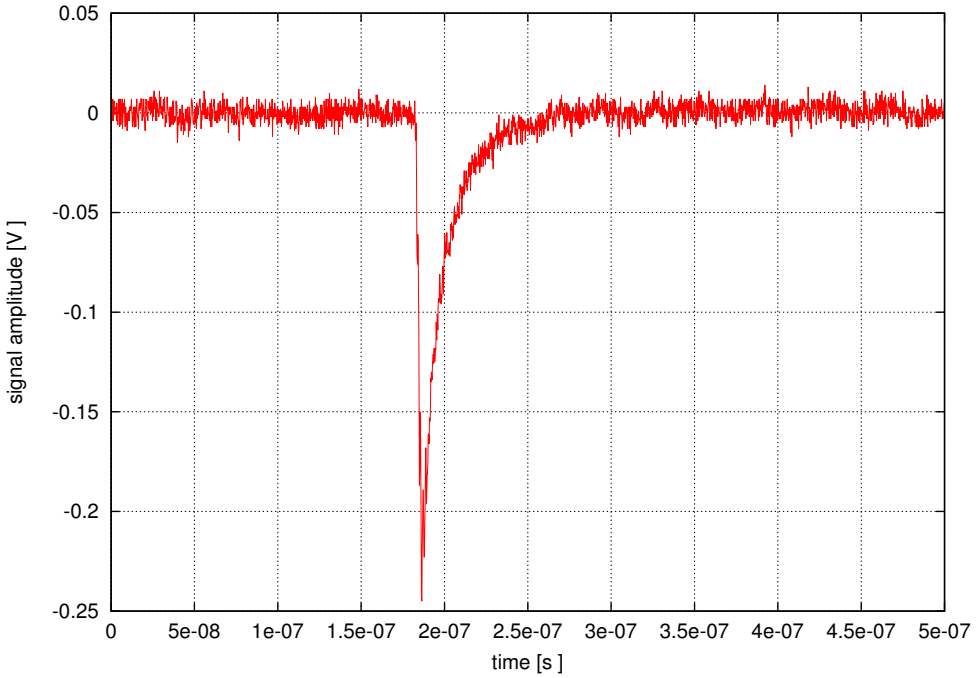

Figure 6.8: Output pulse produced by the real circuit when R = 6.8 kΩ and C = 39 pF; digital pulse width is set to 1.25 ns.

Chapter 7

Conclusions

7.1 Summary

The planned upgrade for the HADES spectrometer for the future operation at SIS18 and SIS100 foresees the introduction of an electromagnetic calorimeter. Each module of this detector needs to be calibrated and quality-assessed individually, before and, periodically, during data taking. The basic idea is to build a remotely controllable light pulse system able to deliver signals similar to the ones the detector would produce during standard operation. To drive the light sources, a generator of short pulses is needed.

During this work of thesis an FPGA-based pulse generator has been designed. This digital pulser allows to generate signals with adjustable frequency and pulse width. By using a high performance FPGA, the minimum value of the pulse width is set to 1.25 ns. Such short pulses are exactly what is needed to drive the LEDs to be used in the final set-up for the testing system. Due to the flexibility of the design, any application that does not require such short signals can also benefit from this pulse generator, eventually implementing it in a less performance FPGA, for it is able to generate longer pulses as well. Since the pulse width and the frequency can be set via slow control, the pulser system can be operated remotely, allowing its use during data taking.

Exploiting the results achieved with the digital pulse generator and

combining it with a simple analog board, a hybrid pulse generator has been developed as well. It can produce signals similar in shape to the ones delivered by the ECAL PMTs, characterized by fast rising edge, slow falling edge and amplitude between 0.3 V and 4 V, that can be used to test the front-end board PADIWA AMPS. Furthermore, it can produce more symmetric pulses similar to the ones produced in, for instance, a diamond detector. Despite that, the tests in the laboratory have shown that the circuit is very sensitive to external noise.

As the same electronics (TRB3 (TDCs, control)) and PADIWA (amplification, discrimination) are being used in the development of future detectors for FAIR, experiments such as PANDA and CBM might benefit from the achievements presented in this thesis.

7.2 Outlook

The functionality of the digital design has been succesfully tested in the laboratory but not yet used to drive the LEDs, as planned. The actual test with the modules of the ECAL will require some additional work.
At the moment, the design features only four equal output pulses. The number of outputs has to be increased and possibly some additional features will be added, in order to allow for checking the behaviour of the TDCs.

The hybrid analog pulser is designed to work with very short digital input signals (1 - 2 ns). Therefore a fast FPGA is needed. So far, one of the peripheral FPGAs of the TRB3 has been employed. Since this board is far too big for this purpose, it is foreseen to replace it with a smaller one, and have an Add-On board providing the analog components and the required number of pins, that will make the set-up cleaner, hopefully reducing the noise and allowing for quantitative measurements.
Some tests on the PADIWA AMPS using the hybrid pulser have started and will be completed in the next future.

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List of Acronyms

AGS Alternating Gradient Synchrotron

ASIC Application Specific Integrated Circuit

Bevalac Billions of eV Synchrotron joined to the SuperHILAC linear accelerator as an injector for heavy ions

BNL Brookhaven National Laboratory

CAD Computer Aided Design

CBM Compressed Baryonic Matter

CERN Centre Européen pour la Recherche Nucléaire

COSY COoler SYnchrotron

DAQ Data AcQuisition

DDR Double Data Rate

DIRC Detection of Internally Reflected Cherenkov light

DLL Delay-Locked Loop

DRAM Dyamic Random Access Memory

DSP Digital Signal Processors

ECAL Electromagnetic CALorimeter

FAIR Facility for Antiproton and Ion Research

FPGA Field Programmable Gate Array

FSM Finite State Machine

FTDI Future Technology Devices International

GSI GSI Helmholtzzentrum für Schwerionenforschung

HADES High Acceptance DiElectron Spectrometer

HDL Hardware Description Language

I2C Inter-Integrated Circuit

JTAG Joint Test Action Group

LED Light Emitting Diode

LHC Large Hadron Collider

LPDDR Low Power Double Data Rate

LSB Least Significant Bit

LUT Look-up table

LVDS Low Voltage Differential Signaling

MDC Multiwire Drift Chamber

META Multiplicity and Electron Trigger Array

MVD Micro Vertex Detector

OPAL Omni-Purpose Apparatus for LEP

PADIWA PAnda-DIrc-WAsa

PANDA antiProton ANnihilation at DArmstadt

PLL Phased-Locked Loop

PMT PhotoMultiplier Tube

QCD Quantum Chromo Dynamics

QGP Quark-Gluon Plasma

RAM Random Access Memory

RHIC Relativistic Heavy Ion Collider

RICH Ring Image CHerenkov

RPC Resistive Plate Chambers

SIS SchwerIonen Synchrotron

SPI Service Provider Interface

SPS Super Proton Synchrotron

SRAM Static Random Access Memory

TAPS Two-Arm Photon Spectrometer

TDC Time-to-Digital Converter

TOF Time-Of-Flight

TQFP Thin Quad Flat Pack

TRB3 Trigger and Read-out Board version 3

TTL Transistor-Transistor Logic

VHDL Very High Speed Integrated Circuits Hardware Description Language

VHSIC Very High Speed Integrated Circuits